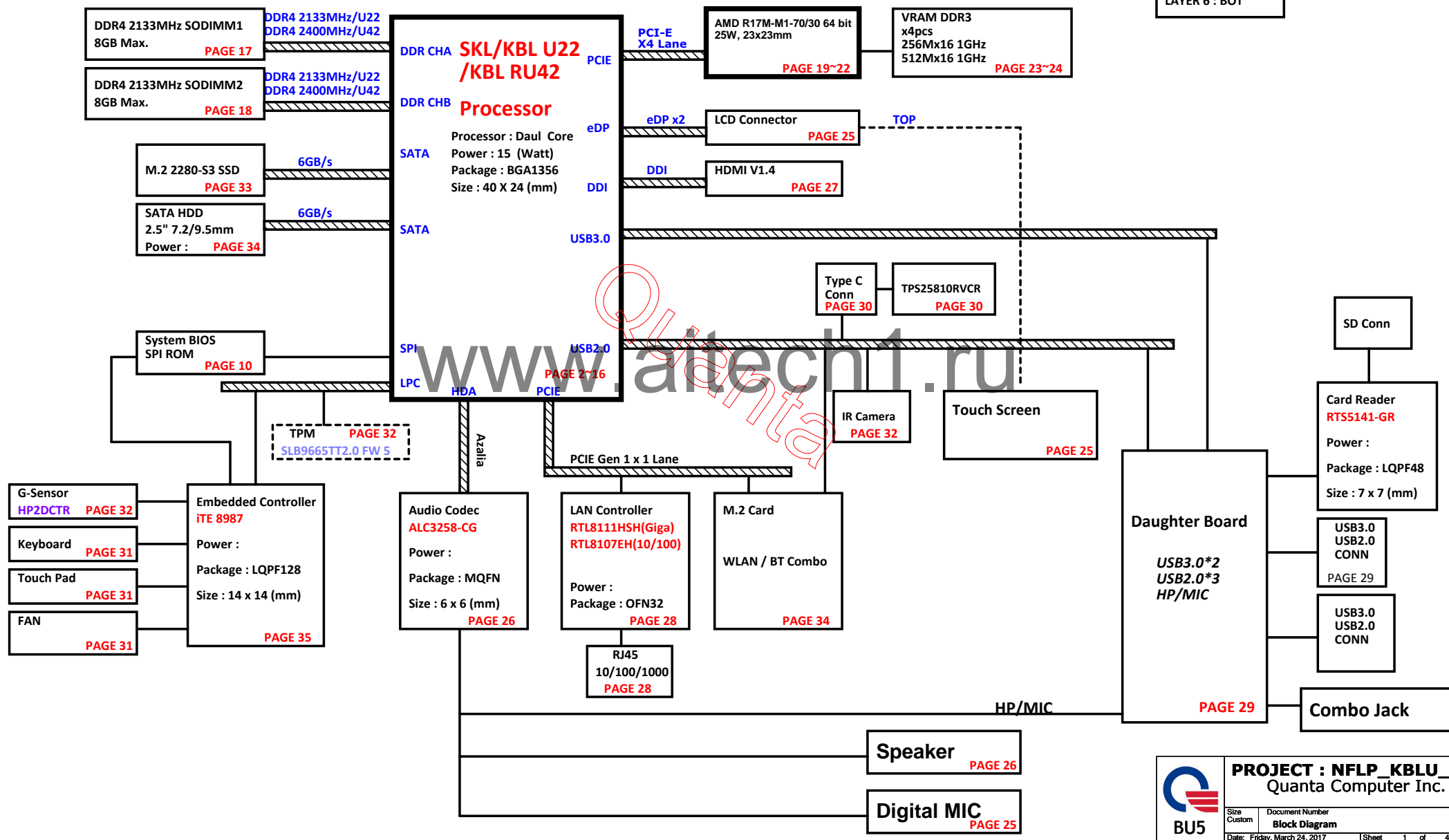


# NFL\_1SPD DIS (14/15")

## Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : BOT



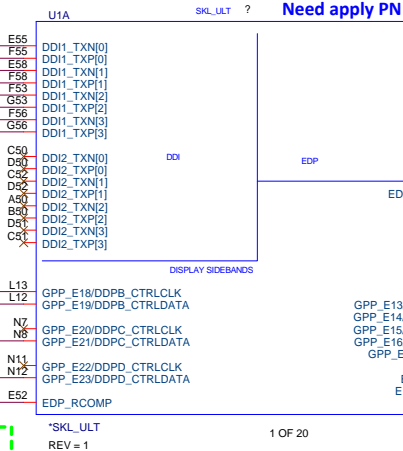
PROJECT : NFLP\_KBLU\_DR  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Friday, March 24, 2017	Sheet 1 of 49	

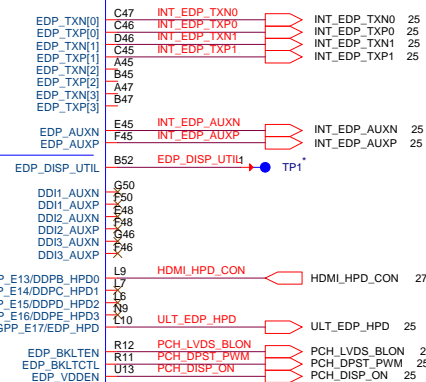
+3V 4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48  
+1.0V 4,6,35,40  
+VCCSTPLL 4,5,6,9,40,41

## HDMI

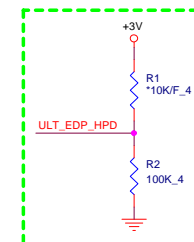
27 IN\_D2#  
27 IN\_D2  
27 IN\_D1#  
27 IN\_D1  
27 IN\_D0#  
27 IN\_D0  
27 IN\_CLK#  
27 IN\_CLK



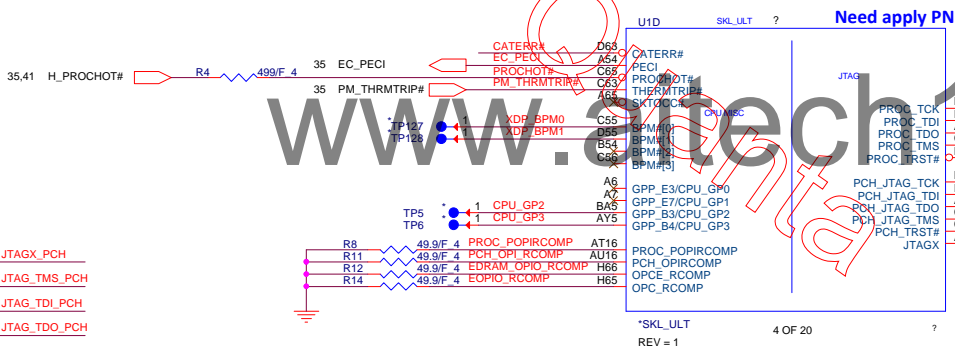
Justsurport FHD 1920x1080

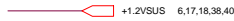


Reserve EDP\_HPD opposites circuit!



eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms





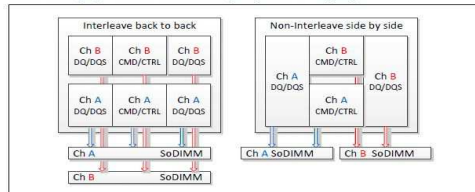
Need apply PN



\*SKL\_ULT

2 OF 20

### Interleave (IL) and Non-Interleave (NIL) Modes Mapping



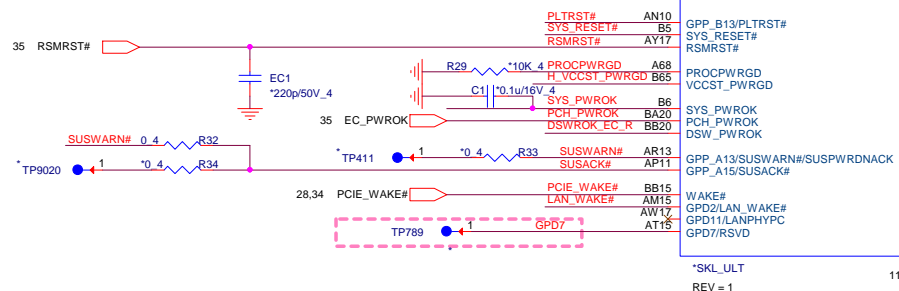
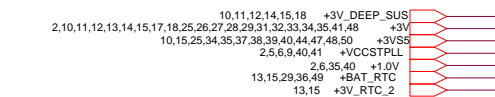
SKL\_UM

Need apply PN

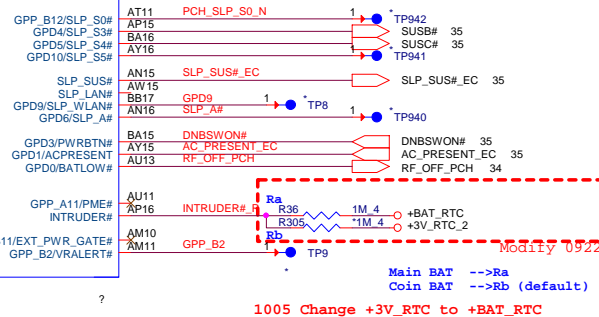


\*SKL\_ULT

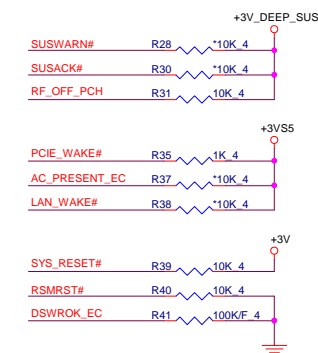
3 OF 20



Need apply PN



## PCH Pull-high/low(CLG)



## For DS3 Sequence

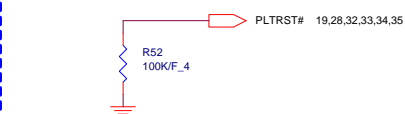
For DS3 --&gt; Ra

Non-DS3 --&gt; Rb

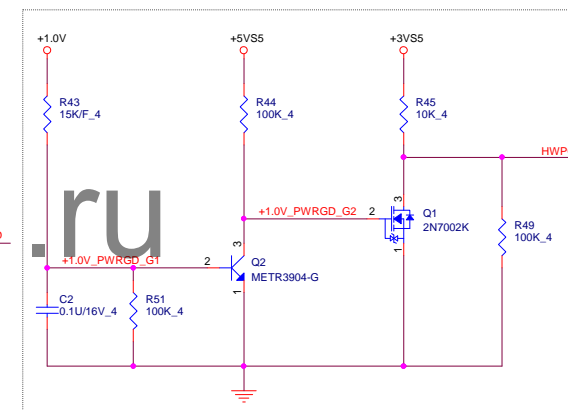
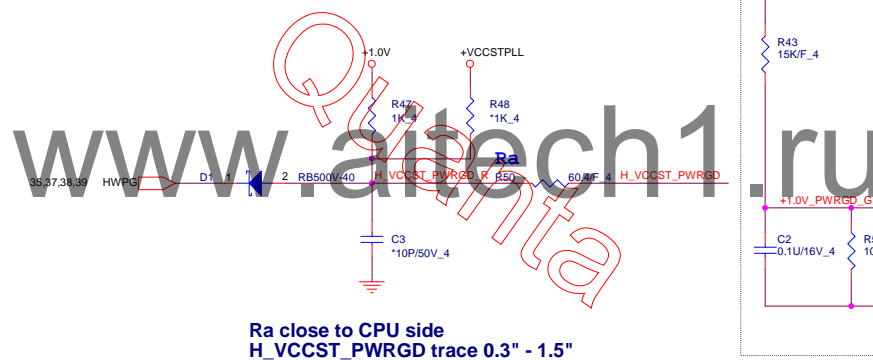
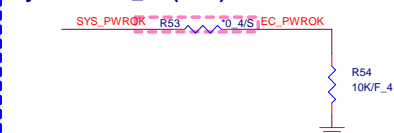


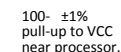
## PLTRST#(CLG)

Check Rise/Fall time less than 100ns

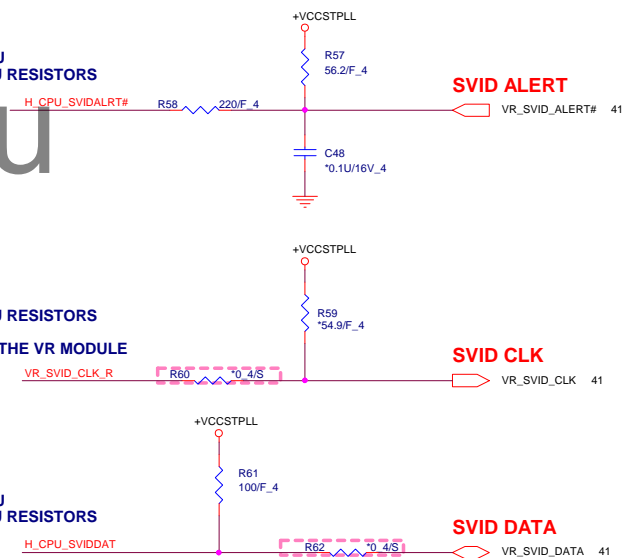


## System PWR\_OK(CLG)






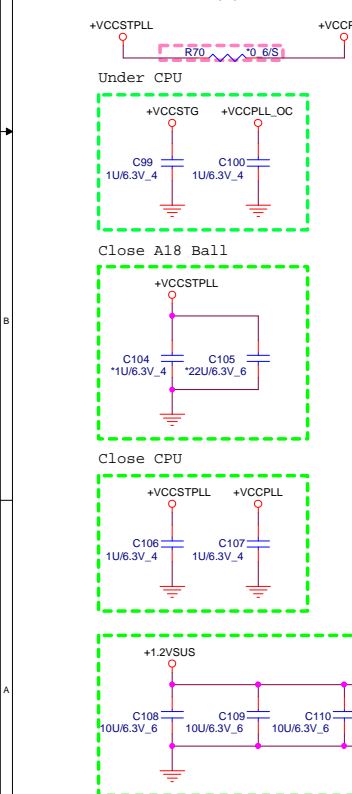
**CLOSE TO CPU  
PLACE THE PU RESISTORS**



**PLACE THE PU RESISTORS  
CLOSE TO VR  
PULL UP IS IN THE VR MODULE**

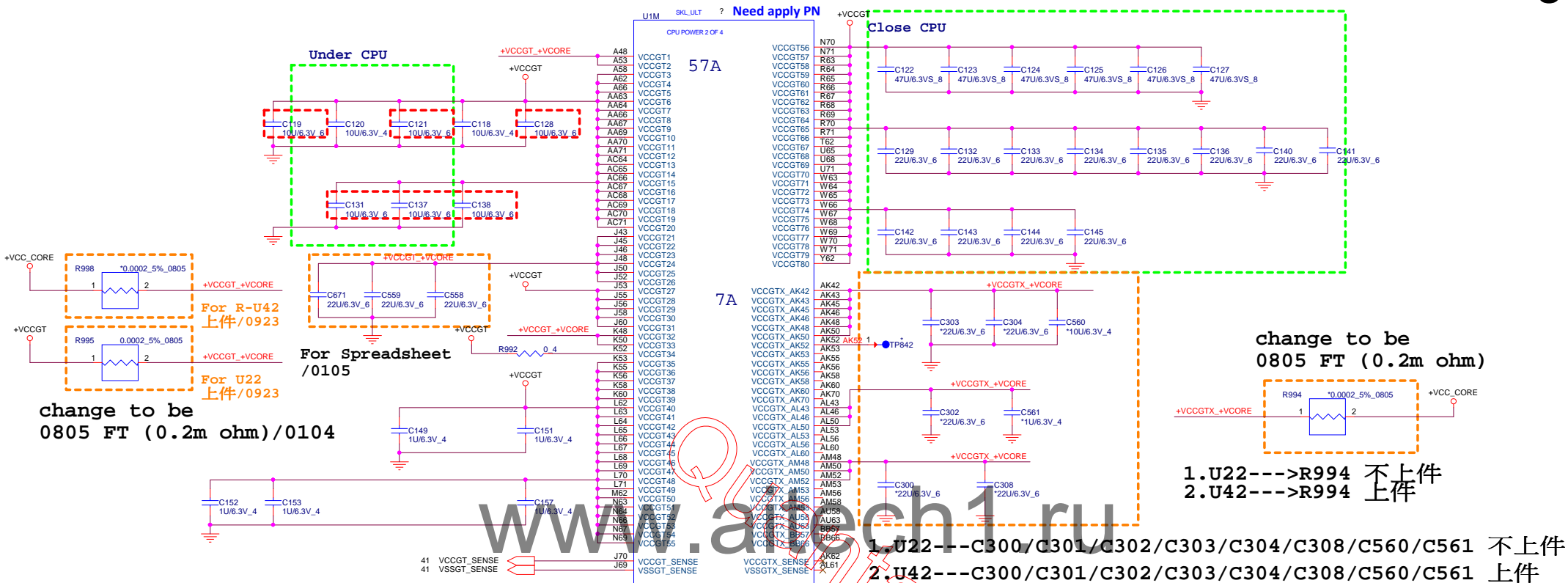
**CLOSE TO CPU  
PLACE THE PU RESISTORS**

	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>05 -- SKYLAKE 4/15 (POWER-1)</b>	Rev 1A
Date: Friday, March 24, 2017		Sheet 5 of 49	

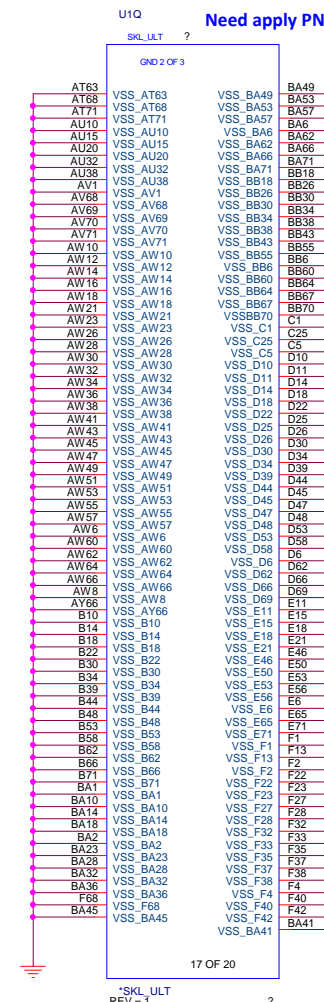
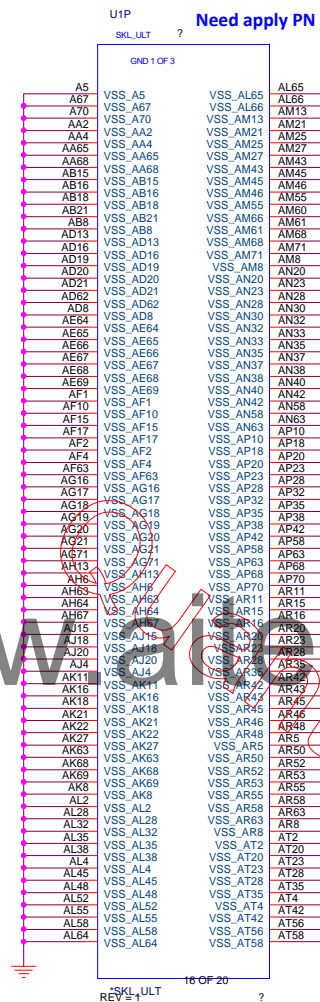
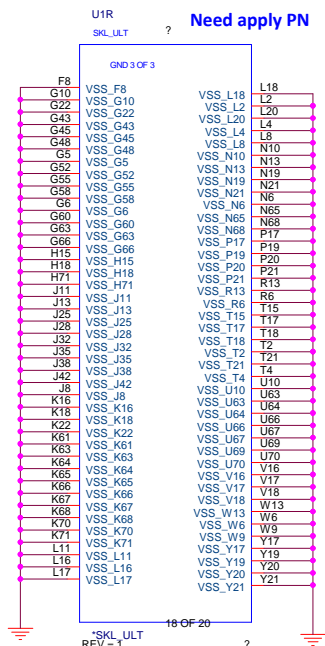


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCI<sub>O</sub></sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



+VCCGT 41,43  
+VCC\_CORE 5,41,42  
+1.2VUS 3,6,17,18,38,40

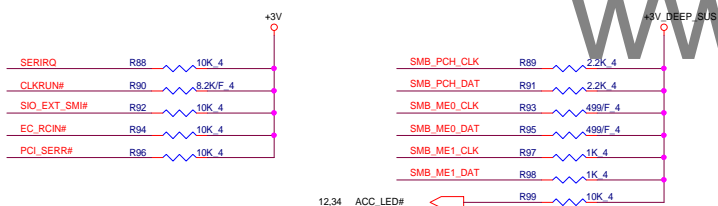


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	



## PCH SPI ROM (CLG)

Vendor	Size	P/N
EON	8MB	AKE3EZNO0Q1 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFPON07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGNO0Q1 (GD25B64BSIGR)
Socket		DFHS08FS023

```

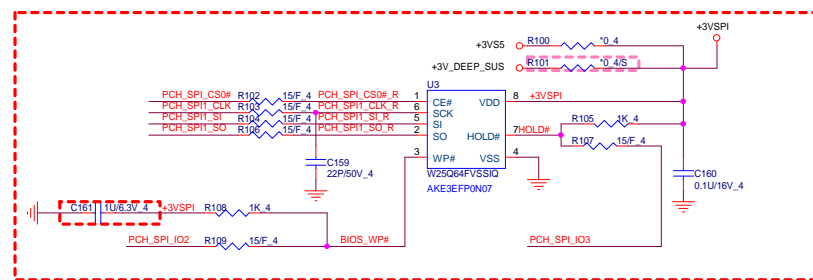
35 PCH_SPI_CS0#_R
35 PCH_SPI1_CLK_R
35 PCH_SPI1_SI_R
35 PCH_SPI1_SO_R

```

need place to TOP

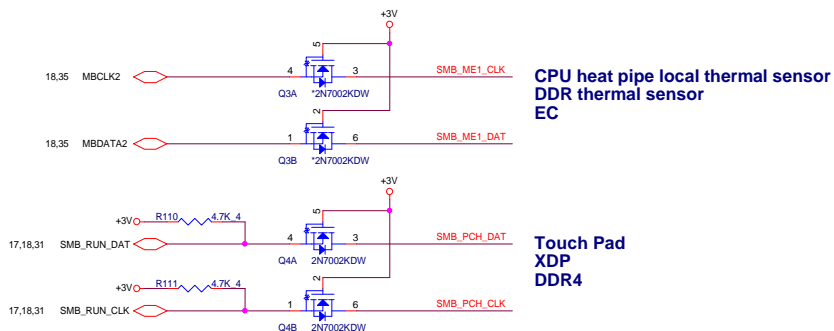
TP17	1	PCH_SPI_CS0#_R
TP18	1	PCH_SPI_CLK_R
TP19	1	PCH_SPI_SI_R
TP20	1	PCH_SPI_SO_R
TP21	1	BIOS_WP#
TP22	1	HOLD#

## PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

### SMBus/Pull-up(CLG)



# Functional Strap Definitions

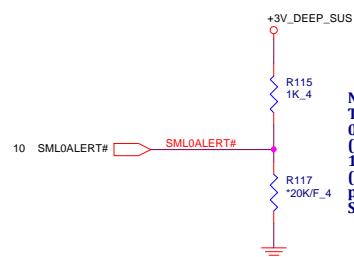
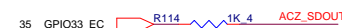
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



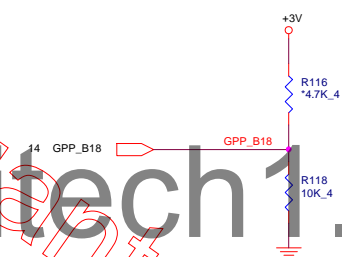
**TOP SWAP OVERRIDE**  
HIGH - TOP SWAP ENABLE  
LOW-DISABLED  
HIGH: LPC SELECTED FOR SYSTEM FLASH  
WEAK INTERNAL PD



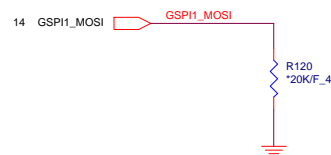
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



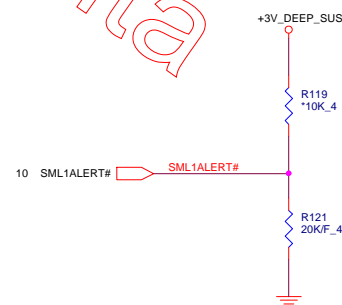
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



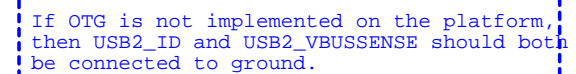
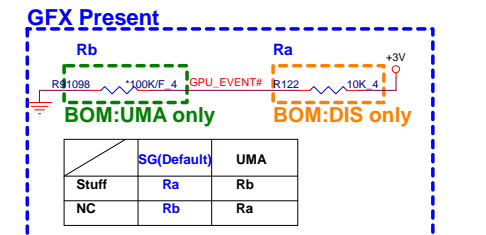
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10      Boot BIOS Destination**  
0            SPI  
1            LPC

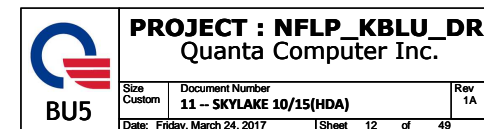


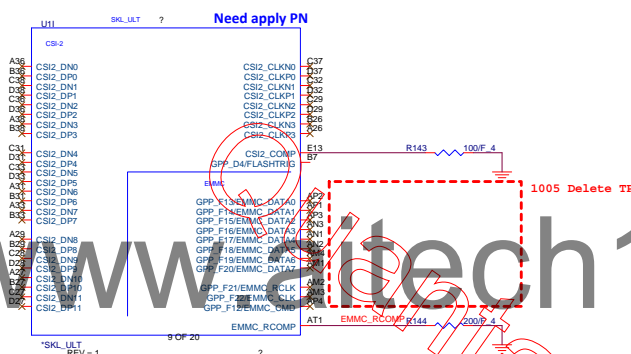
**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.



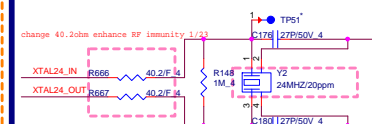
```
GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low
```

USB2.0	Function
PORT-1	USB3.0 Small Board
PORT-2	USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	Cardreader IC
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

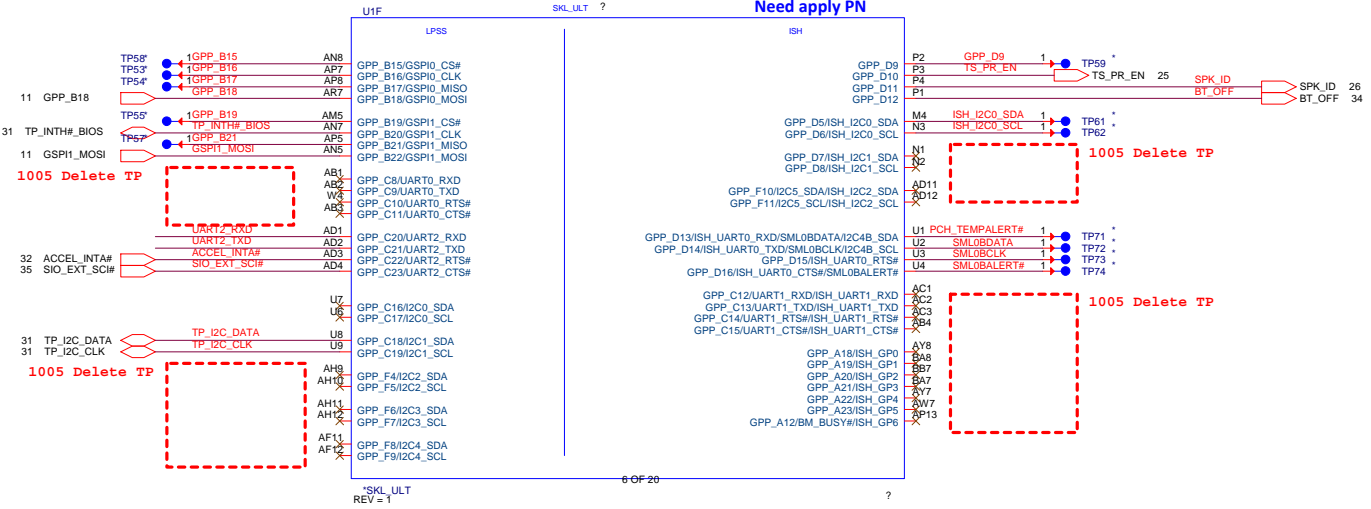
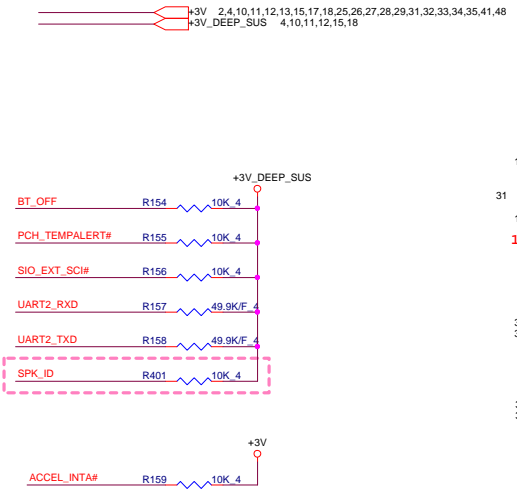


[illegible]

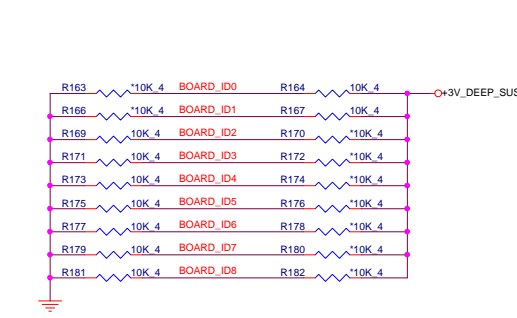
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



Skylake (GPIO)

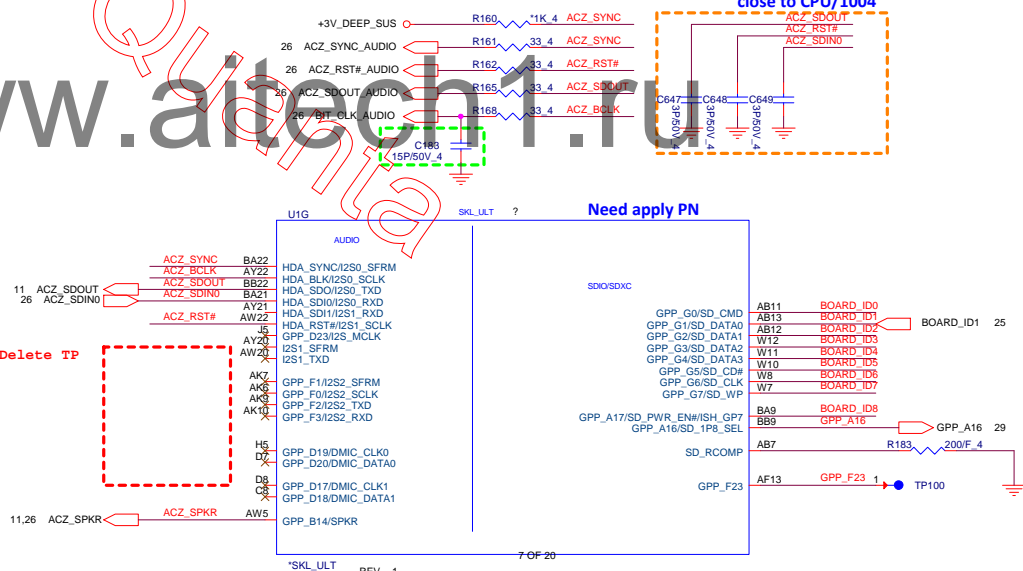



HDA Bus(CLG)



skylake	BOARD_ID[8:6]	BOARD_ID[5]	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7 ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 000)	GPU 0 : AMD 1 : Intel	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	01 14" (14" cable is 00) 01 15" 1SPD 10 17" 11 2SPD	0 : UMA 1 : DIS

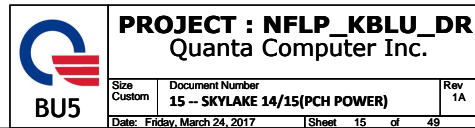
ID1(R167)always 上件






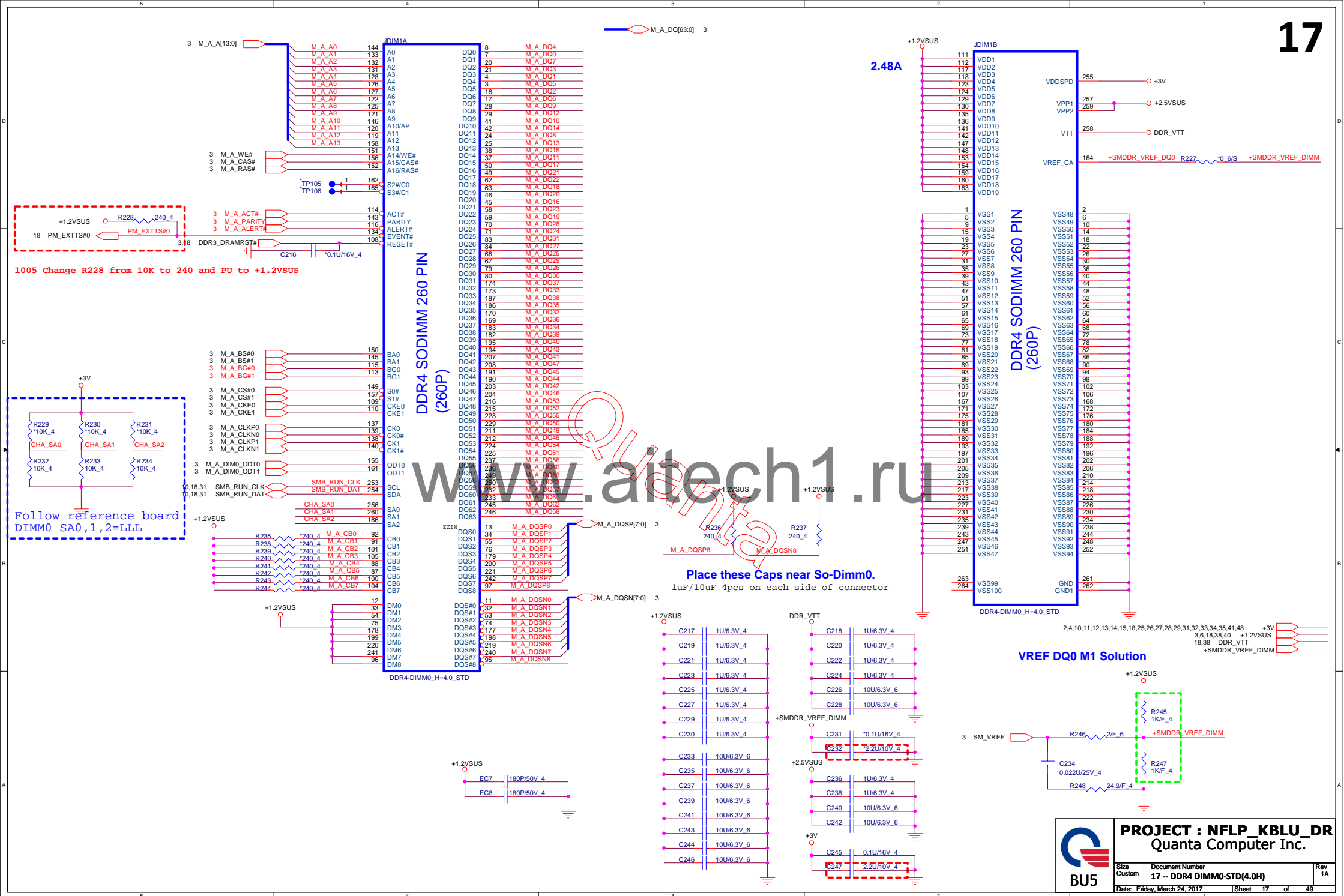
**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

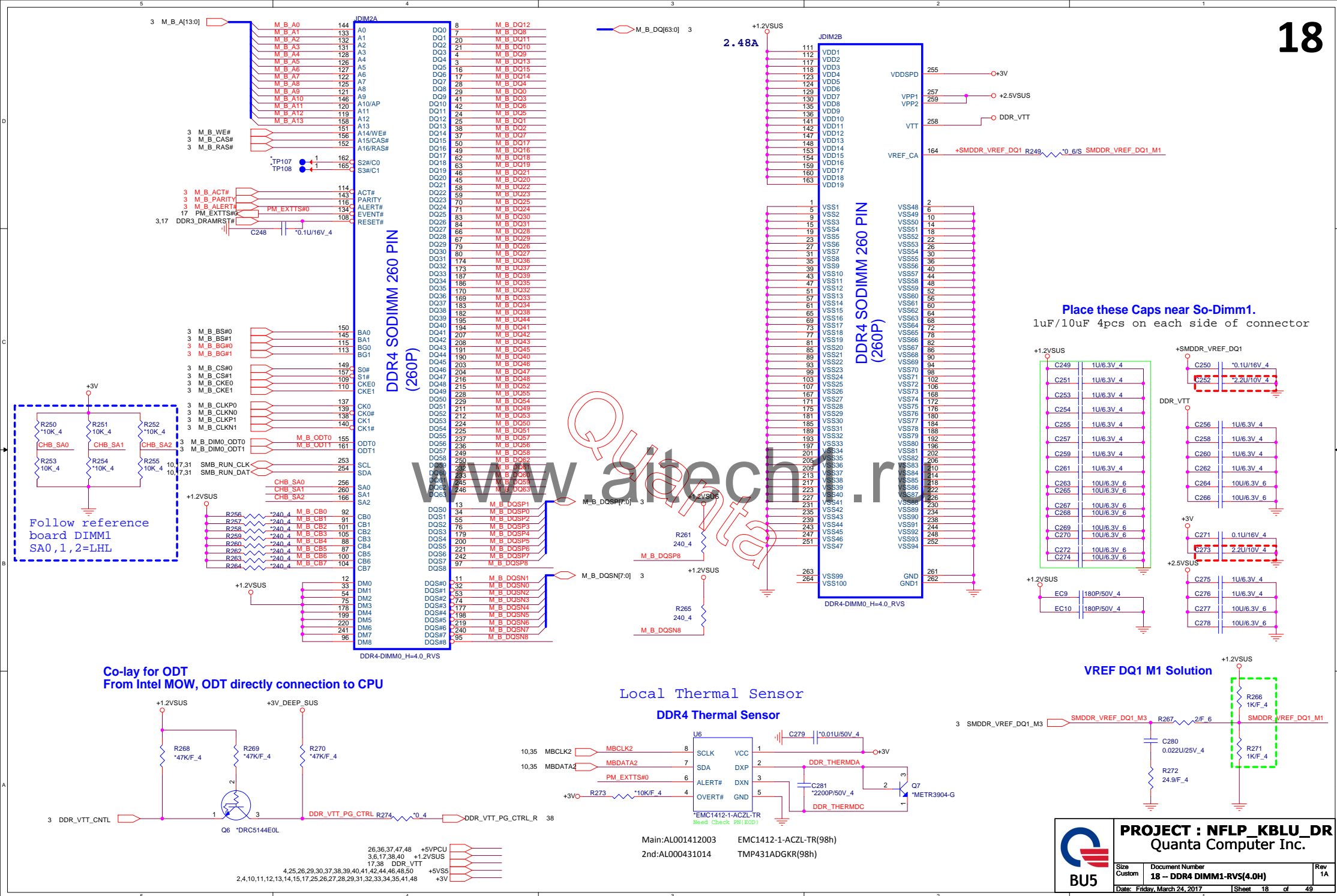
Size Custom	Document Number 14 - SKYLAKE 13/15 (GPIO)	Rev 1A
Date: Friday, March 24, 2017	Sheet 14 of 49	

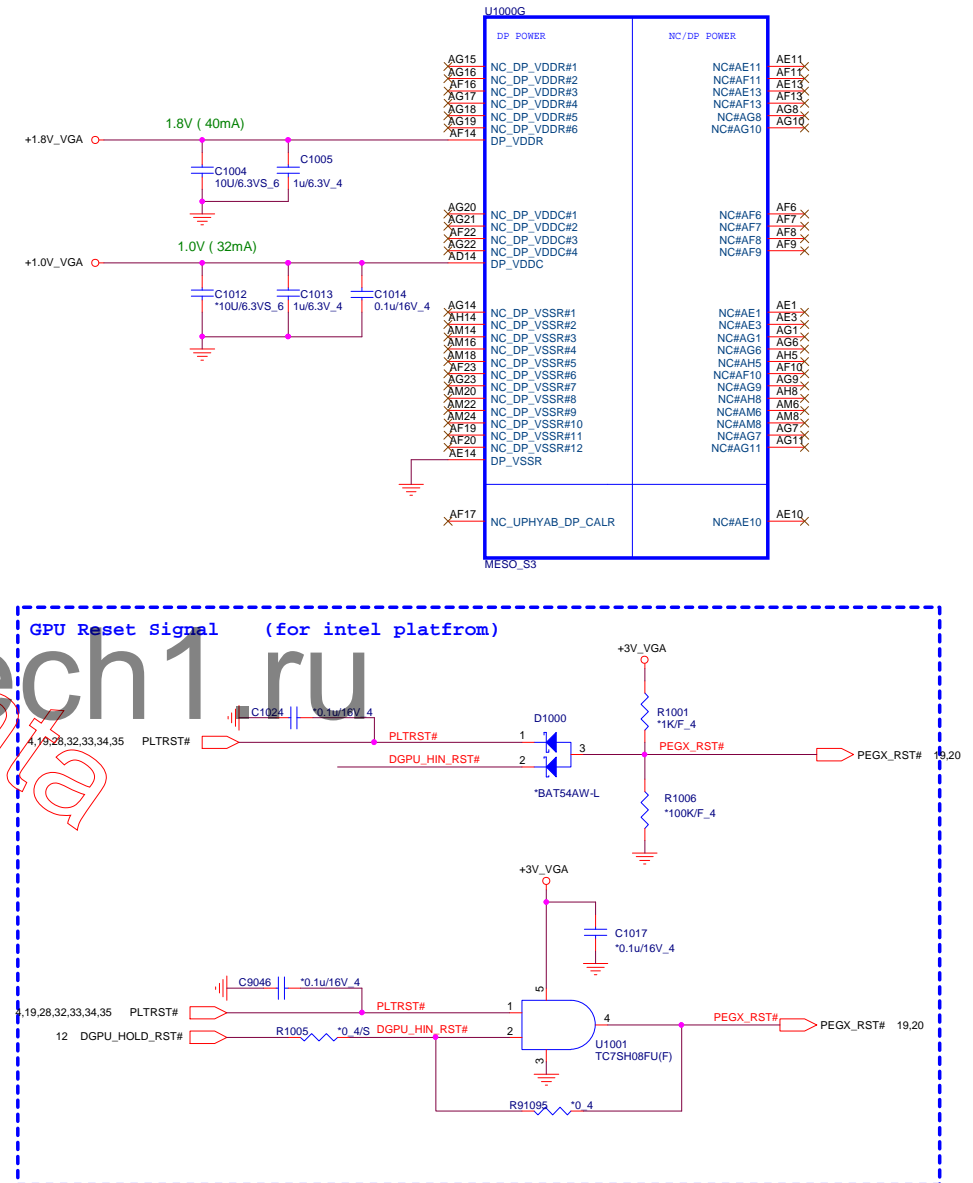
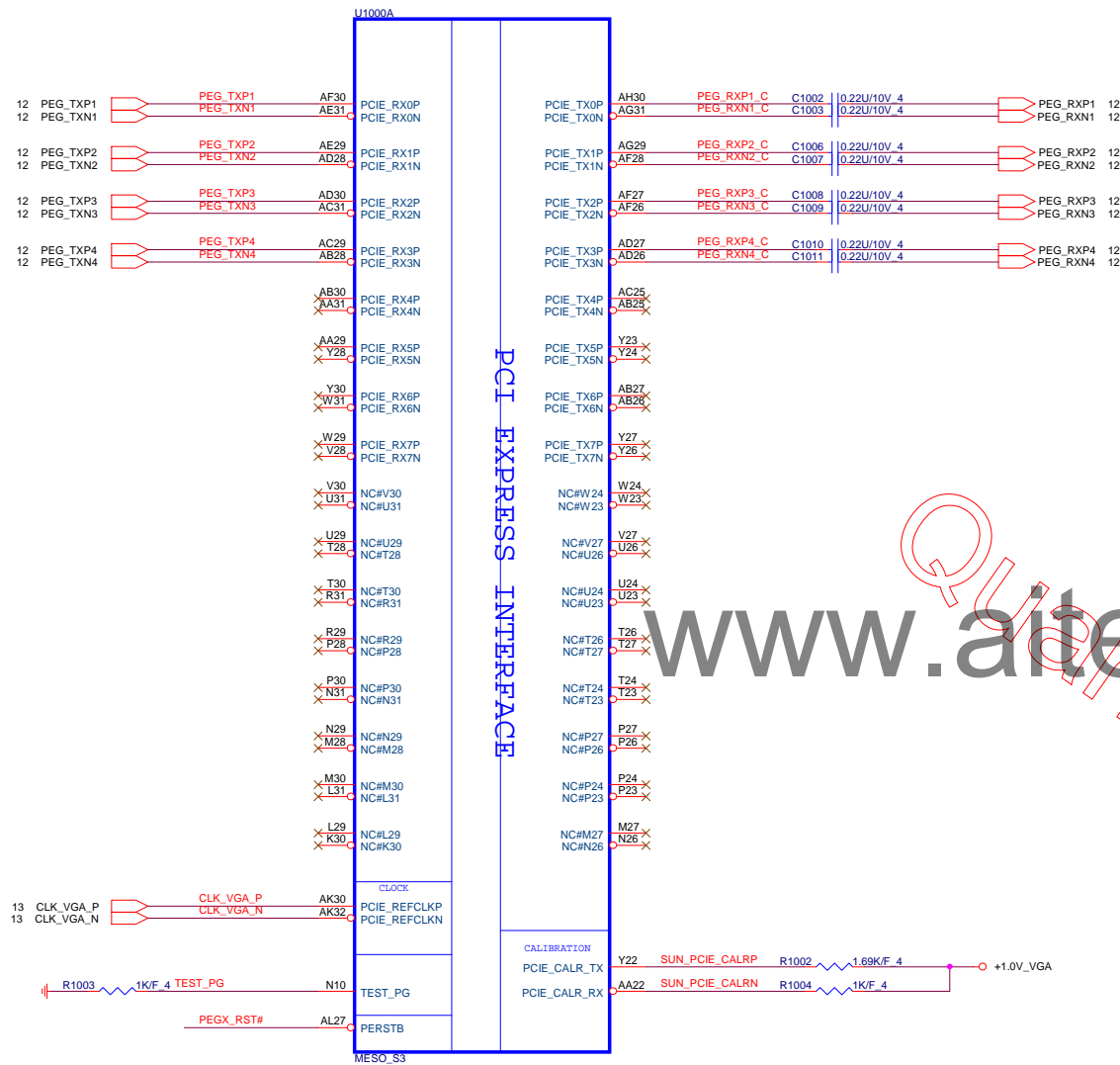


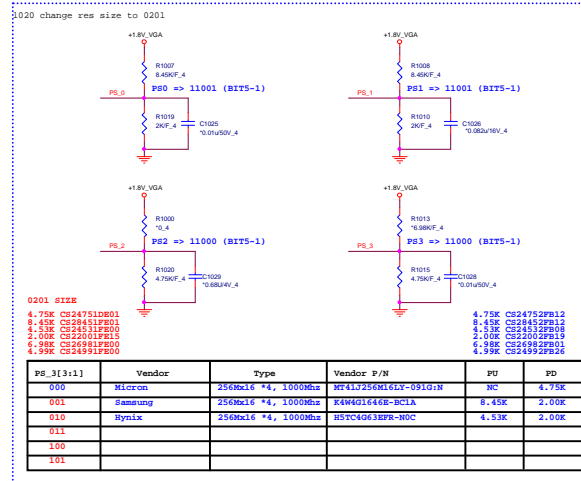
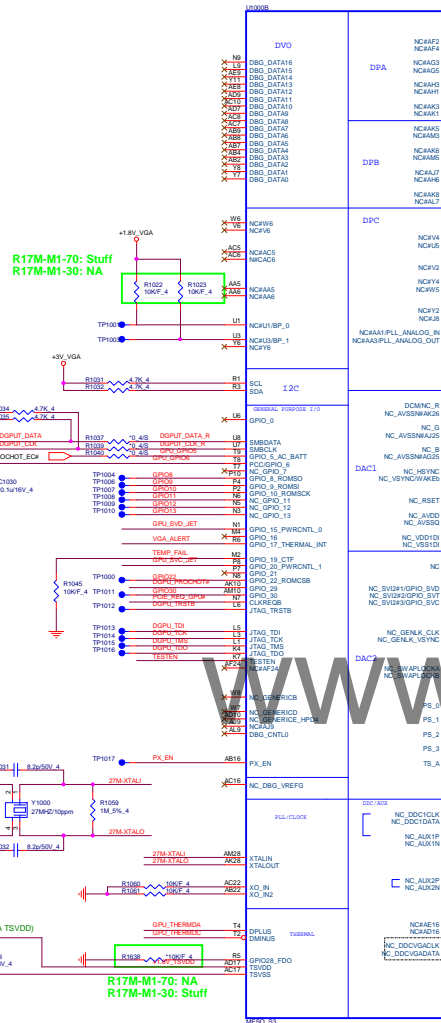
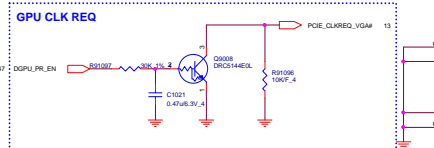
www.aitech1.ru

 <b>BU5</b>	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size	Document Number	Rev
		16 -- SKYLAKE 15/15 XDP&APS *	1A
Date: Friday, March 24, 2017		Sheet	16 of 49



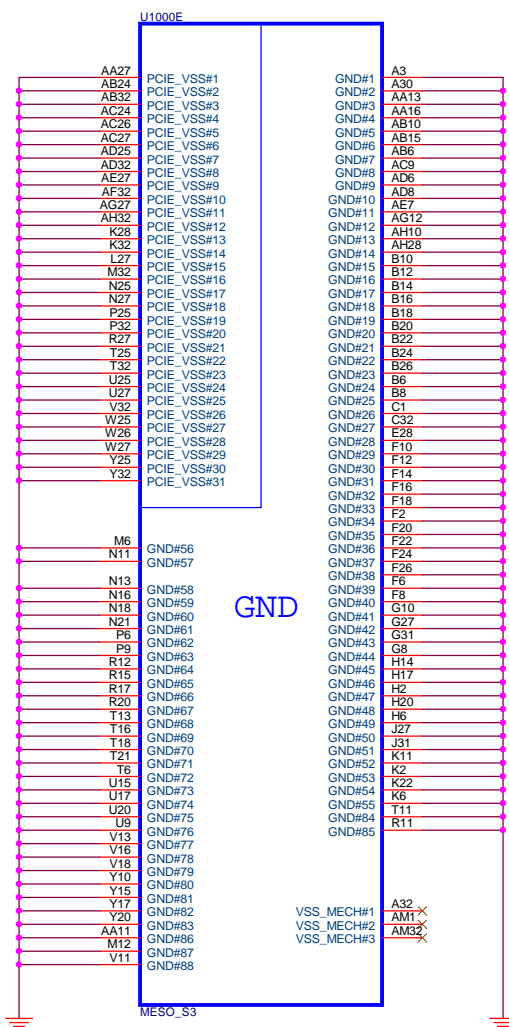




Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0101	ROM_CFG0001	If STRAP BIOS_ROM_EN = 1 If STRAP BIOS_ROM_EN = 0	Designs dependent on the description
PS_0102	ROM_CFG0002	If STRAP BIOS_ROM_EN = 0 ROM_CFG0002 defines the primary memory aperture size. See <a href="#">Legacy Memory Aperture</a> on page 29.	Designs dependent on the description
PS_0103	ROM_CFG0003		
PS_0104	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0105	Reserved		1
PS_0111	STRAP_BIF_GEN_A	1 - PCN GEN3 capability. 0 - PCN GEN3 is supported. Determine whether or not the PCN reference clock power management capability is supported in the P1 configuration space (available on CLEVER3). 1 - The CLEVER3 power management capability is disabled. 0 - The CLEVER3 power management capability is enabled	Designs dependent on the description
PS_0121	STRAP_BIF_CLK_PEN_EN		0
PS_0131	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_0141	STRAP_TX_CV0_CV1_PULL_DOWN	Control the transmitter full-holding mode. 0 - The transmitter half-on is enabled. 1 - The transmitter full-on is enabled	1
PS_0151	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter de-emphasis. 0 - Tx de-emphasis disabled. 1 - Tx de-emphasis enabled.	Designs dependent on the description
PS_2111	N/A	Reserved.	0
PS_2121	N/A	Reserved.	0
PS_2131	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 - Disable the external BIOS ROM device. 1 - Enable the external BIOS ROM device.	Designs dependent on the description
PS_2141	N/A	Reserved.	1
PS_2151	N/A	Reserved.	1
PS_3101	BOARD_CFG0001	Board configuration related strapings, such as for memory ID	Designs dependent on the description
PS_3121	BOARD_CFG0002		
PS_3131	BOARD_CFG0003		
PS_3141	N/A	Reserved.	1
PS_3151	N/A	Reserved.	1



# **CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS** **ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED,** **THEY MUST NOT CONFLICT DURING RESET**

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 3K RESISTOR  
 X= DESIGN DEPENDANT  
 NA= NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

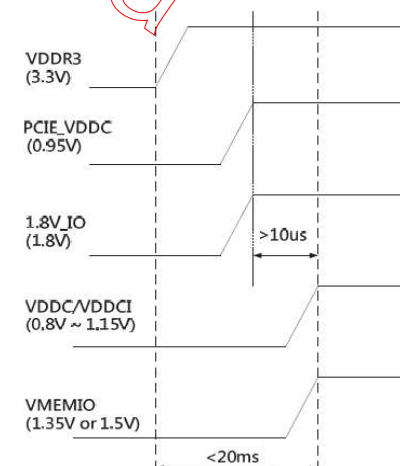
## **NOTE1: AMD RESERVED CONFIGURATION STRAPS**

**ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.**

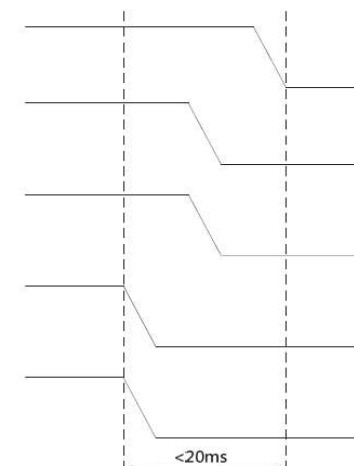
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

## **POWER UP / POWER DOWN SEQUENCE**

### **POWER UP**

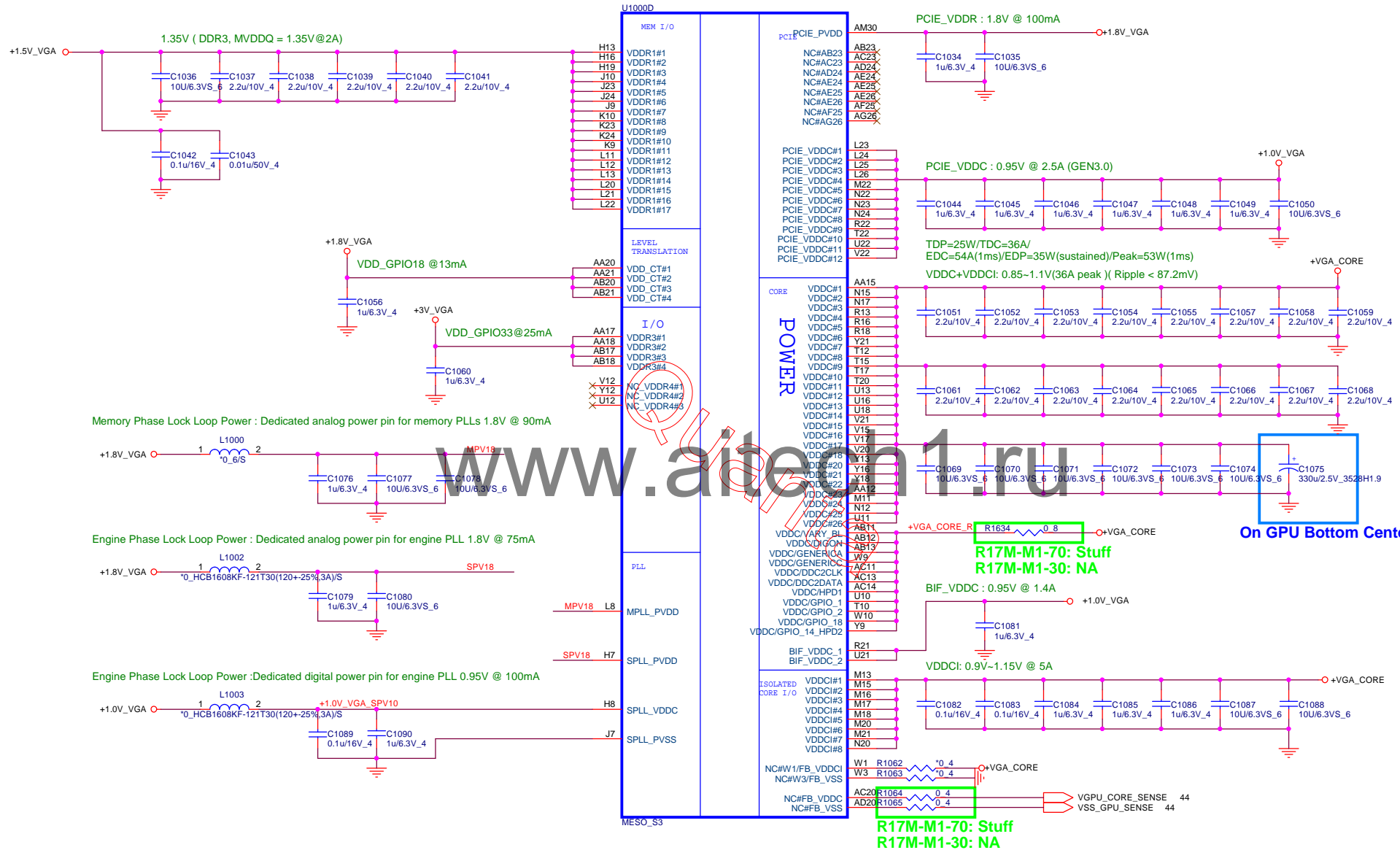


### **POWER DOWN**



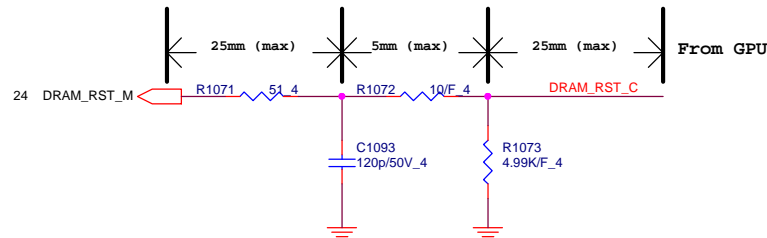
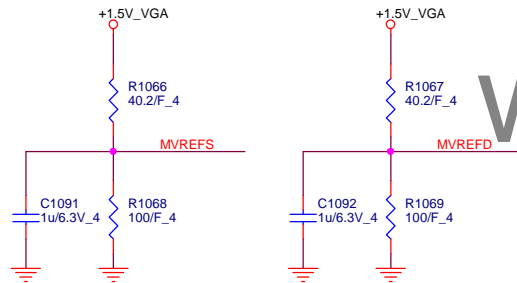
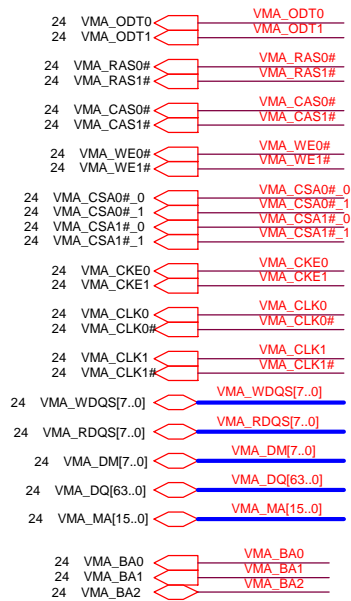
**PROJECT : G54A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>R17M_M2-50_DIS/GND</b>	<b>1A</b>
Date:	Friday, March 24, 2017	Sheet 21 of 48



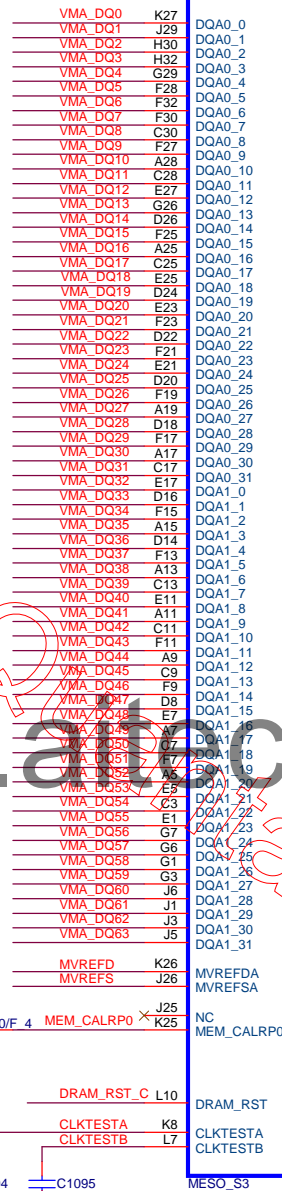
**PROJECT : G54A**  
Quanta Computer Inc.

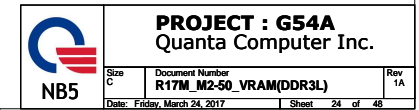
Size	Document Number	Rev
	<b>R17M_M2-50_S3_POWER</b>	1A
Date:	Friday, March 24, 2017	Sheet 22 of 48



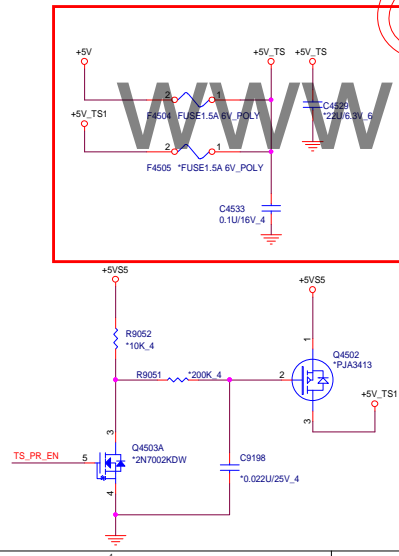
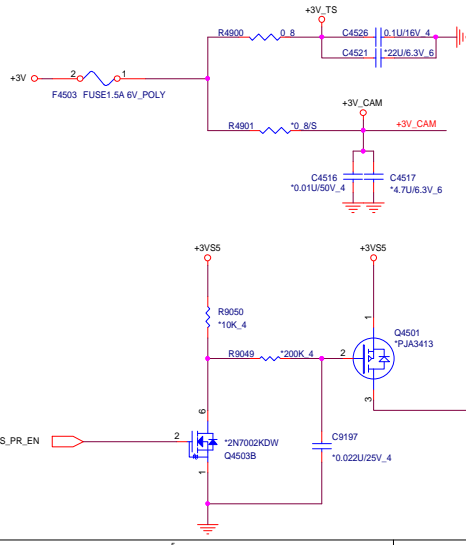
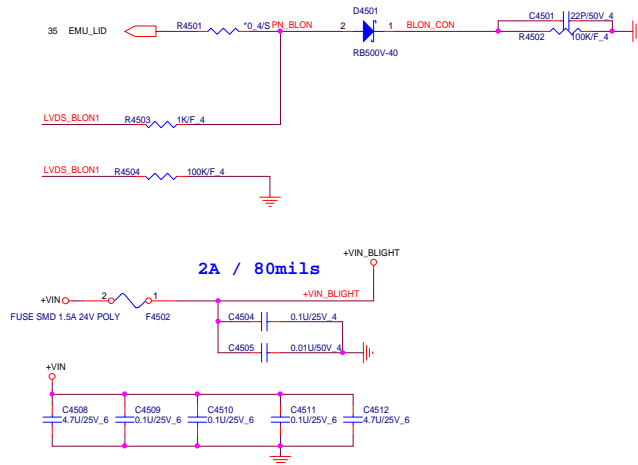
Place all these components very close to GPU. (Within 25mm)  
Keep all component close to each Other. (within 5mm)

This basic topology should be used for DRAM\_RST for DDR3/GDDR5.





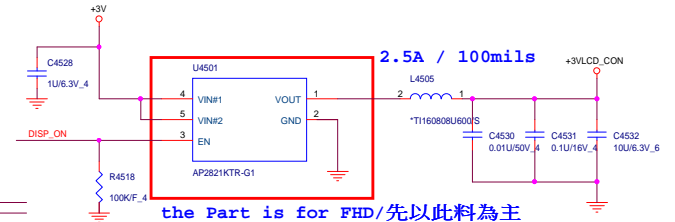
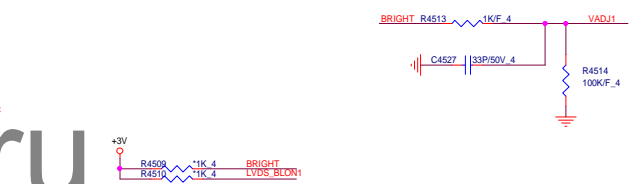
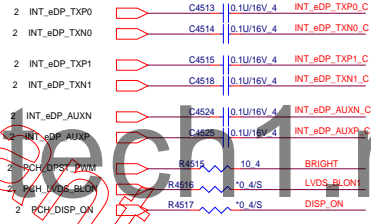
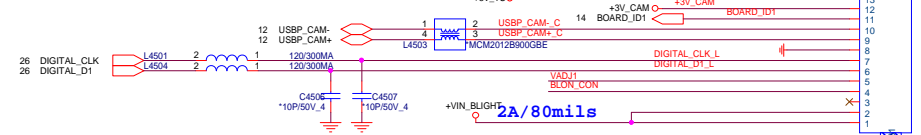
# LID Switch



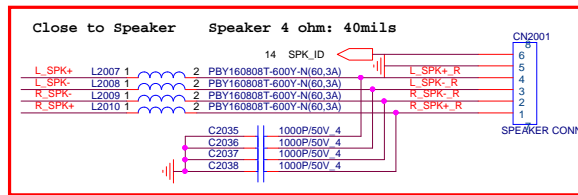
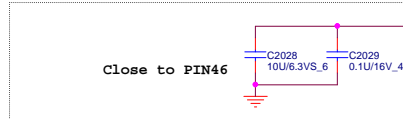
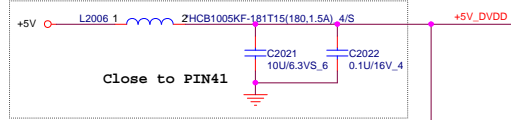
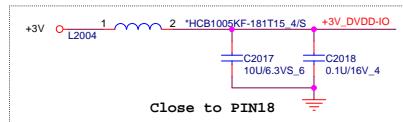
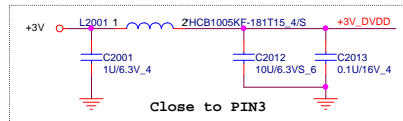
# eDP Conn.



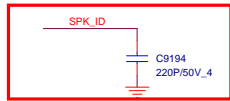
## TS USB Interface



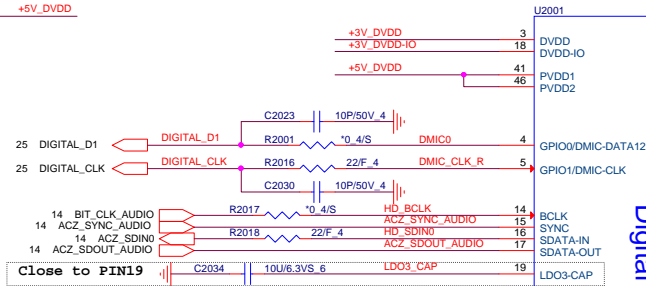
the Part is for FHD/先以此料為主



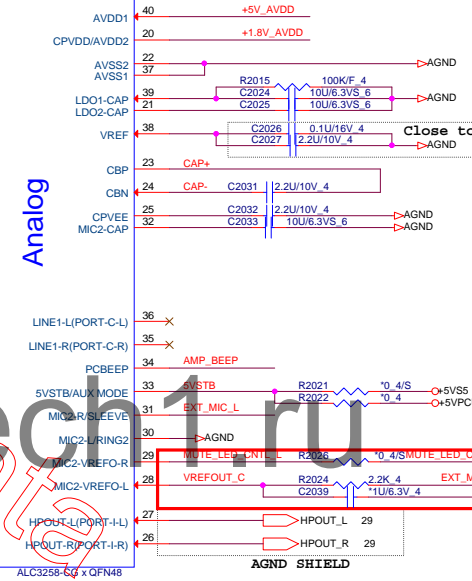
SPK\_ID for Smart amp feature



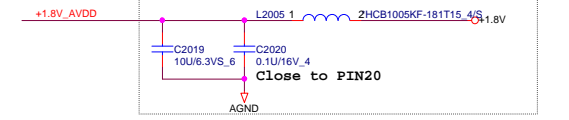
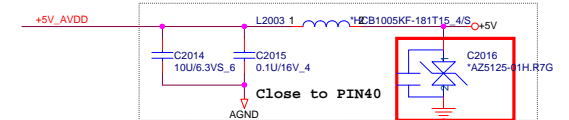
EMI suggestion 0119



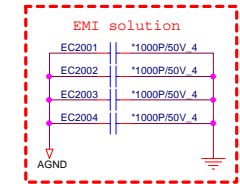
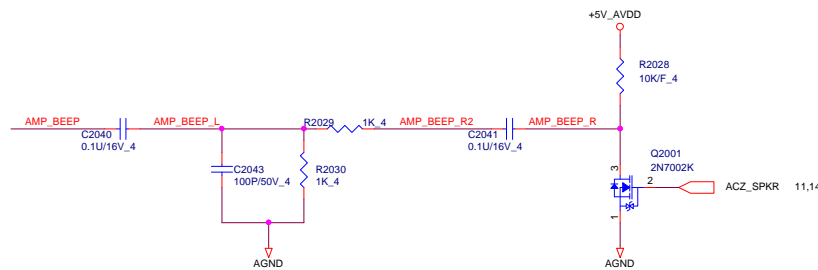
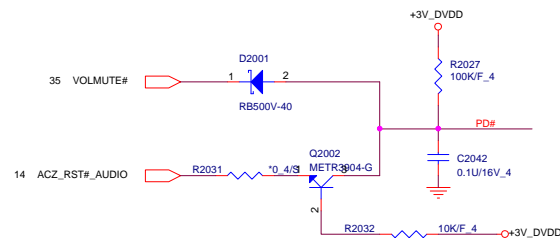
Analog



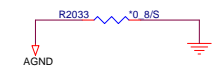
+5V\_AVDD &gt;40mils trace change PN to BC512501Z00 1/23



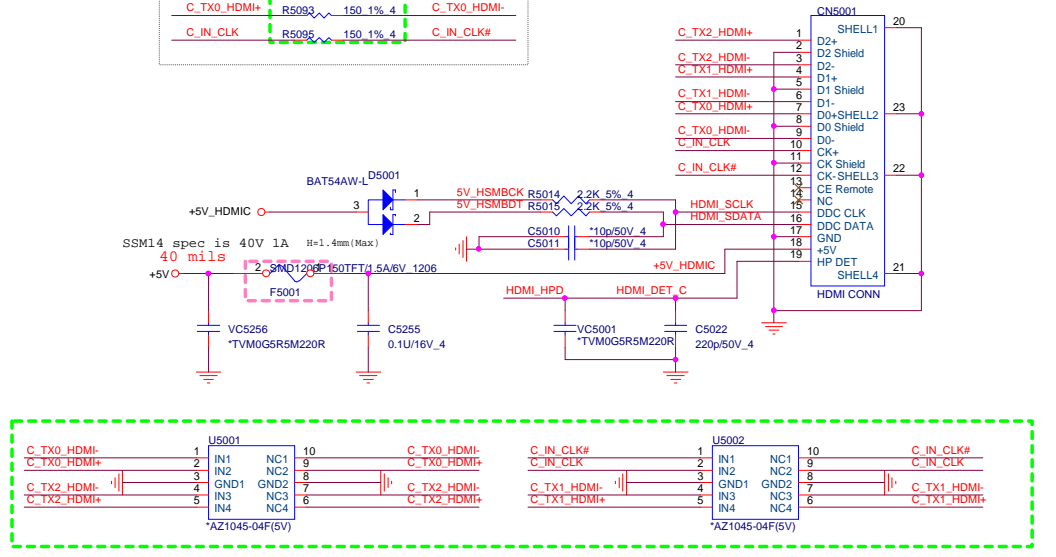
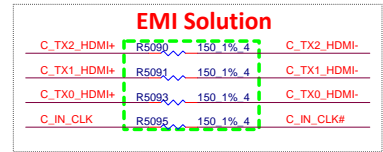
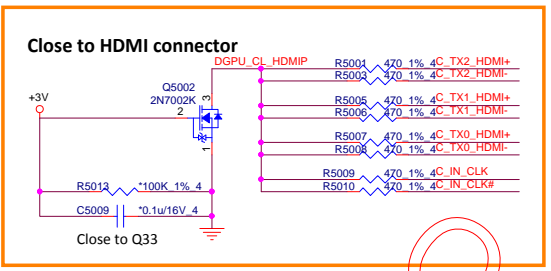
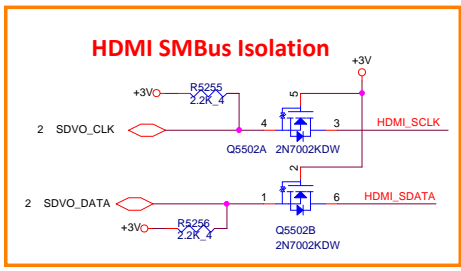
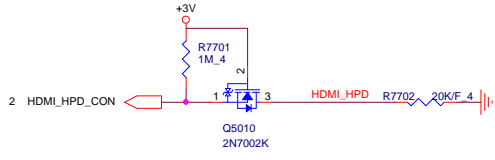
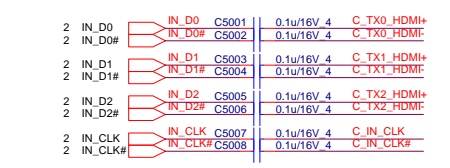
Reserve for codec debug

Mute LED改用Mic2-Vref0-R  
Mic偏壓改用Mic2-Vref0-L

place to under codec

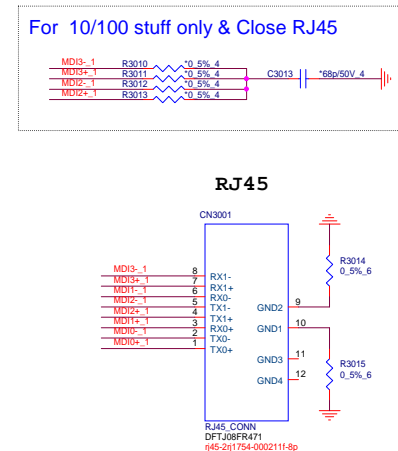
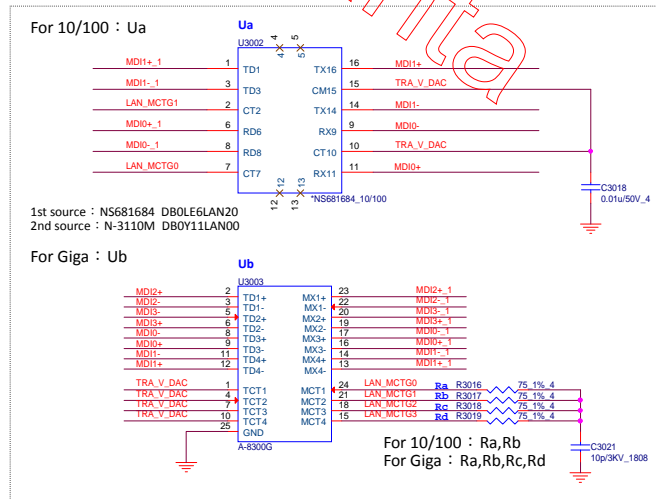
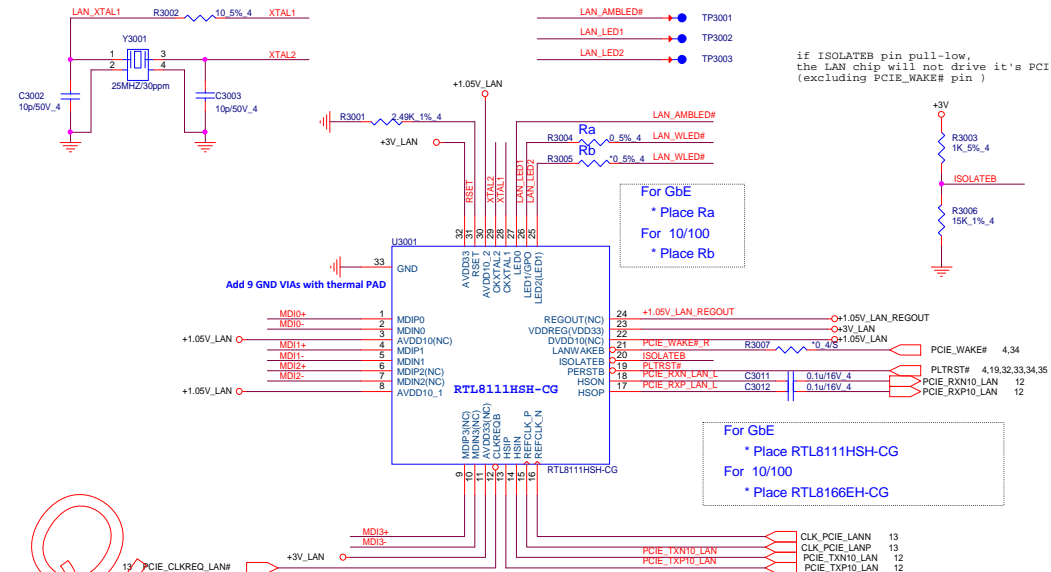
PROJECT : NFLP\_KBLU\_DR  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 -- Codec ALC3258-CG	1A
Date: Friday, March 24, 2017	Sheet 26 of 49	



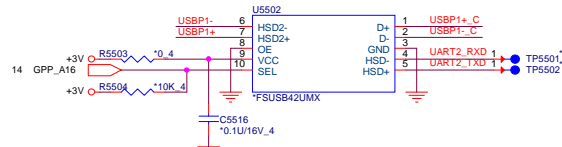
Head Phone out

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12.29 USBP1- R5502 \*0.4 USBP1- C  
12.29 USBP1+ R5501 \*0.4 USBP1+ C

## UART for Win7 WHQL DEBUG



Place Back to Back La

USB3.0

reserve for re-driver un-stuff 01/18

USB3.0

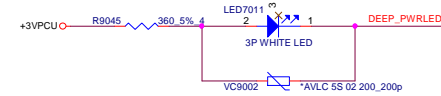
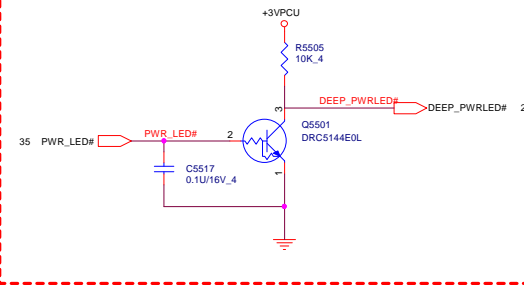
reserve for re-driver un-stuff 01/18

Layout Notes:  
Stubs Trace less than 150mil

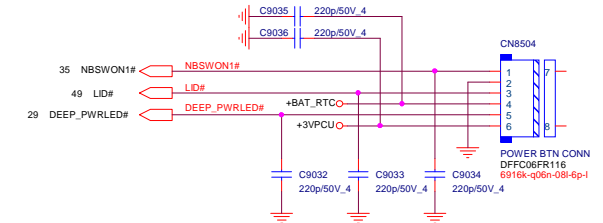
Layout Notes:  
Stubs Trace less than 150mil

## Daughter Board

1123 Add PWR LED MOS Circuit

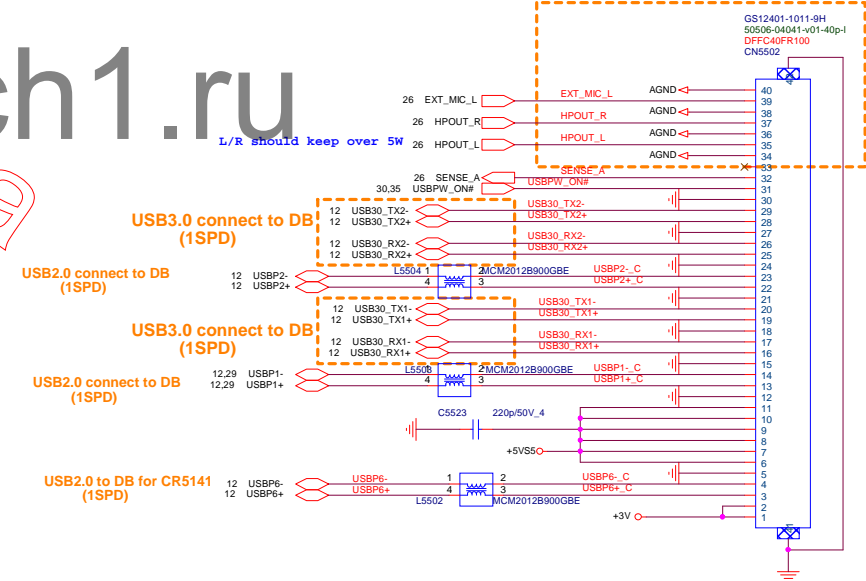


## Power Board



## Daughter Board

For Audio layout routing



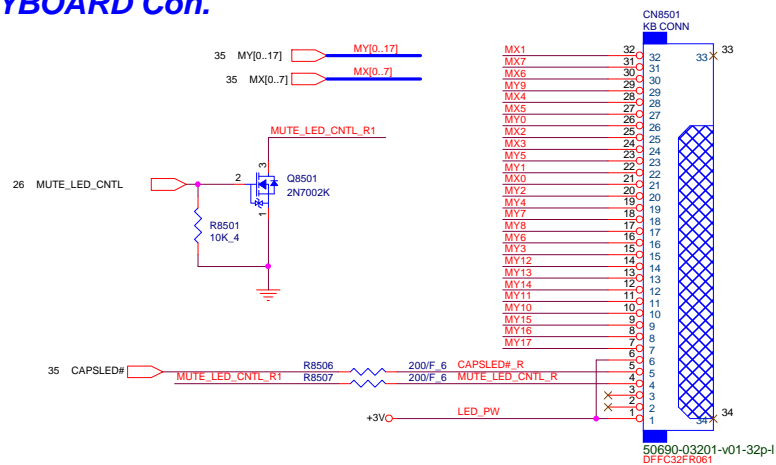
**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

Size Custom Document Number 31 - USB SW & TYPE-C -TPS25810 Rev 1A  
Date: Friday, March 24, 2017 Sheet 29 of 49

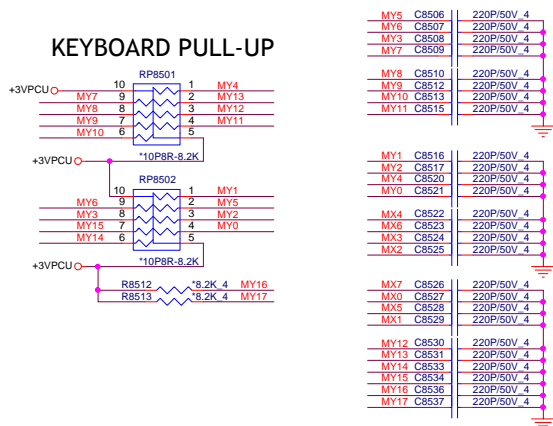
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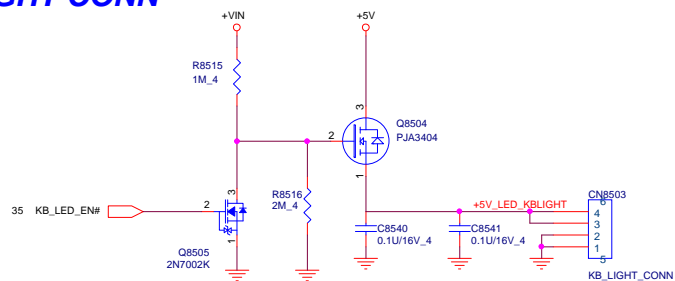
## KEYBOARD Con.



## KEYBOARD PULL-UP

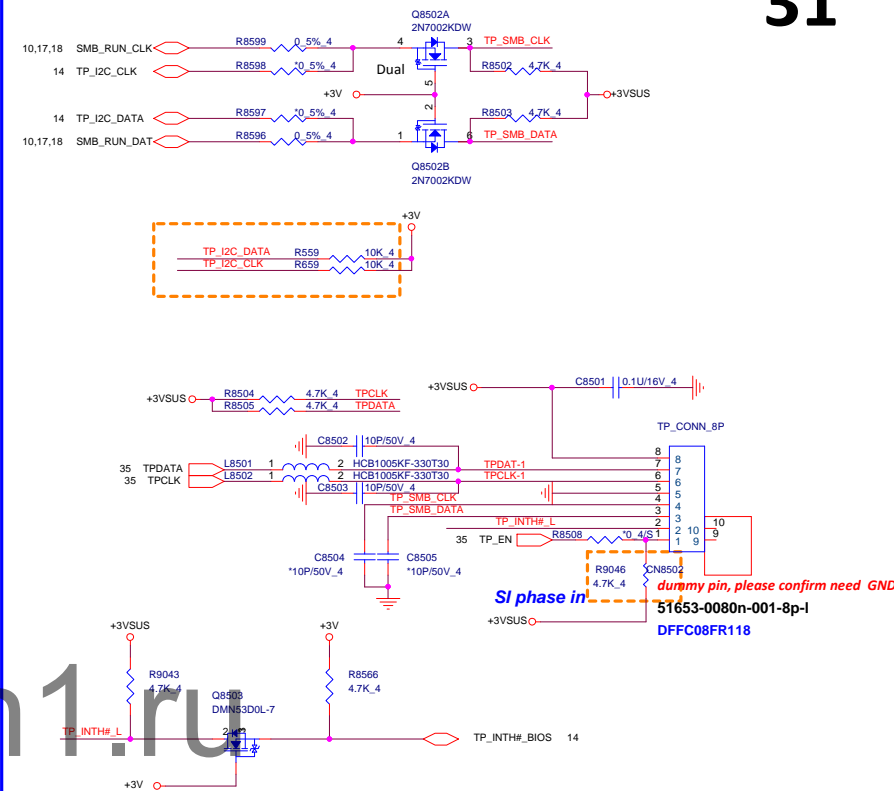


## KB LIGHT CONN

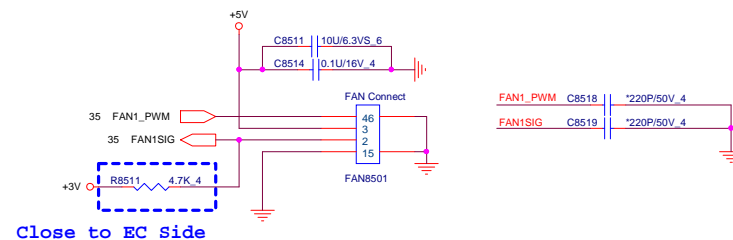


## Touch Pad Connector

31



## FAN



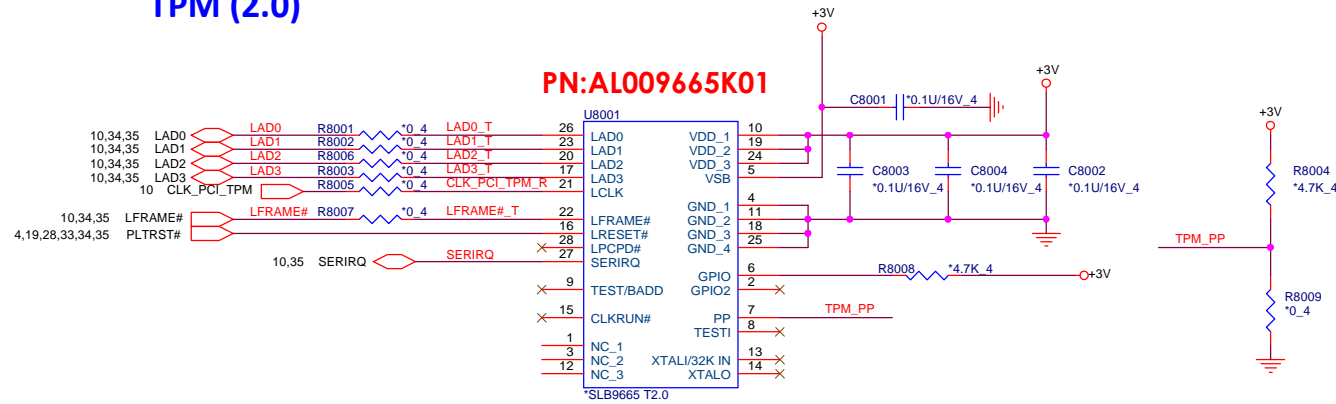
**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 - KB/TP/FAN	1A

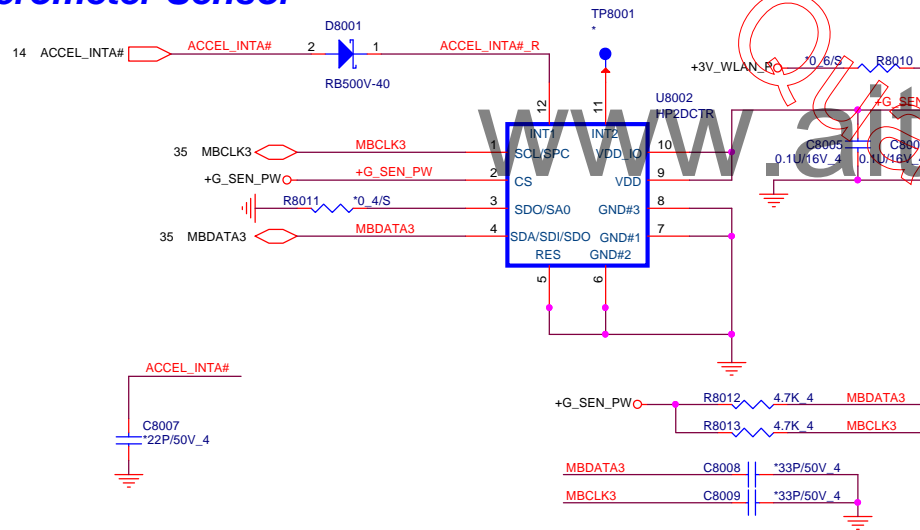
Date: Friday, March 24, 2017 Sheet 31 of 49

## TPM (2.0)

32

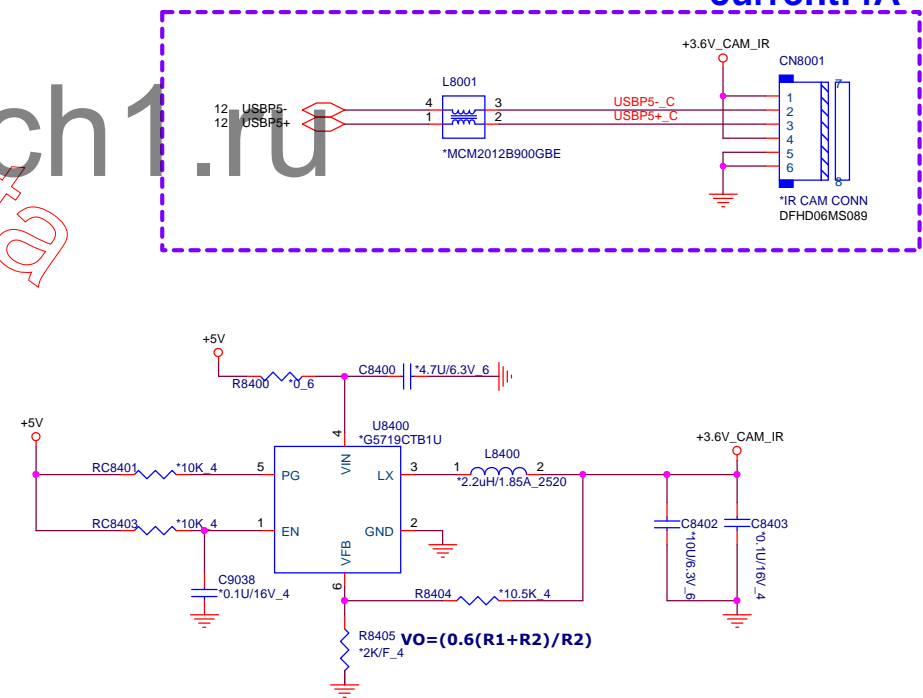


## Accelerometer Sensor



## IR CAM

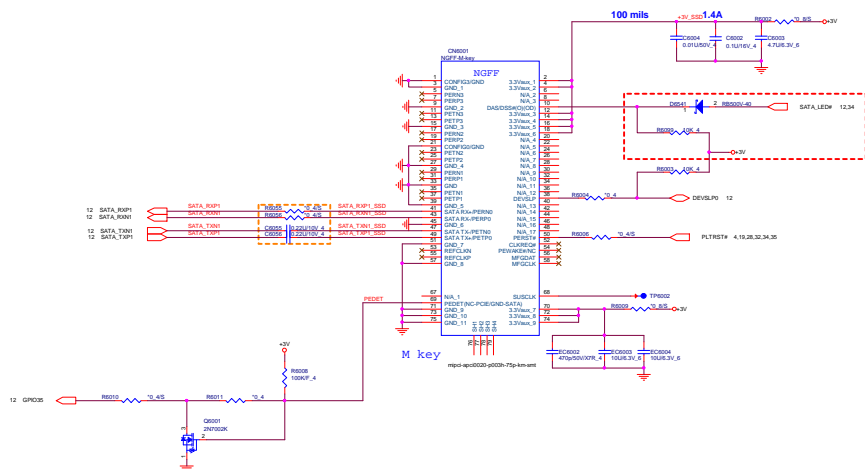
current:4A



**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

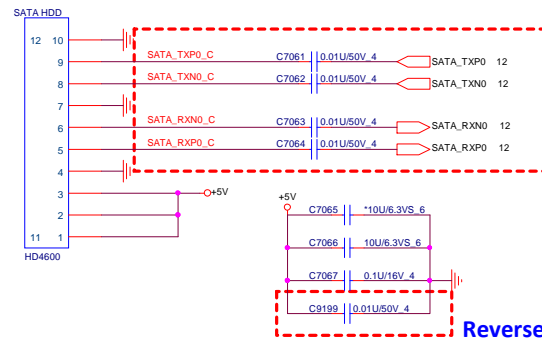
Size	Document Number	Rev
Custom	34 -- TPM/G-Sensor/IR CAM	1A
Date: Friday, March 24, 2017	Sheet	32 of 49

**33**

[illegible]

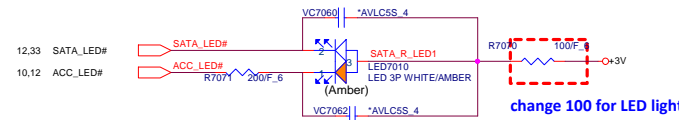
eMMC

## SATA HDD

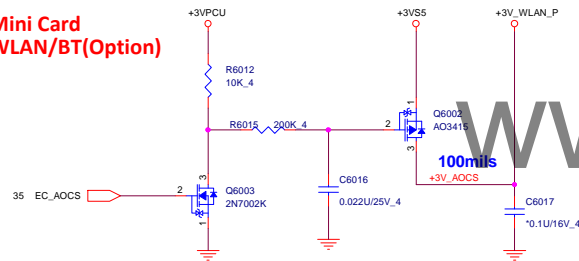


Reverse for ESD

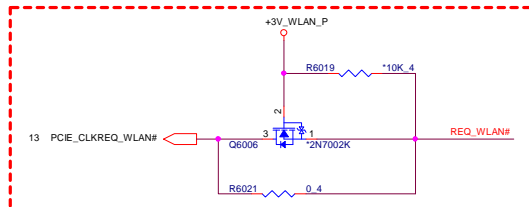
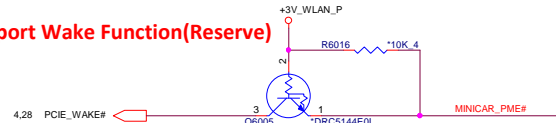
## SATA LED



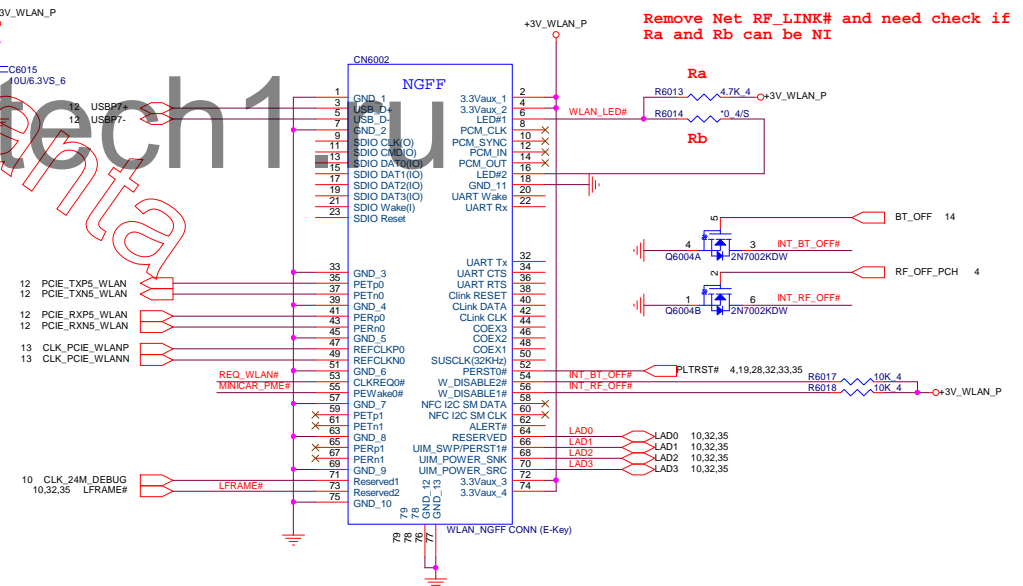
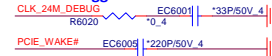
## WLAN

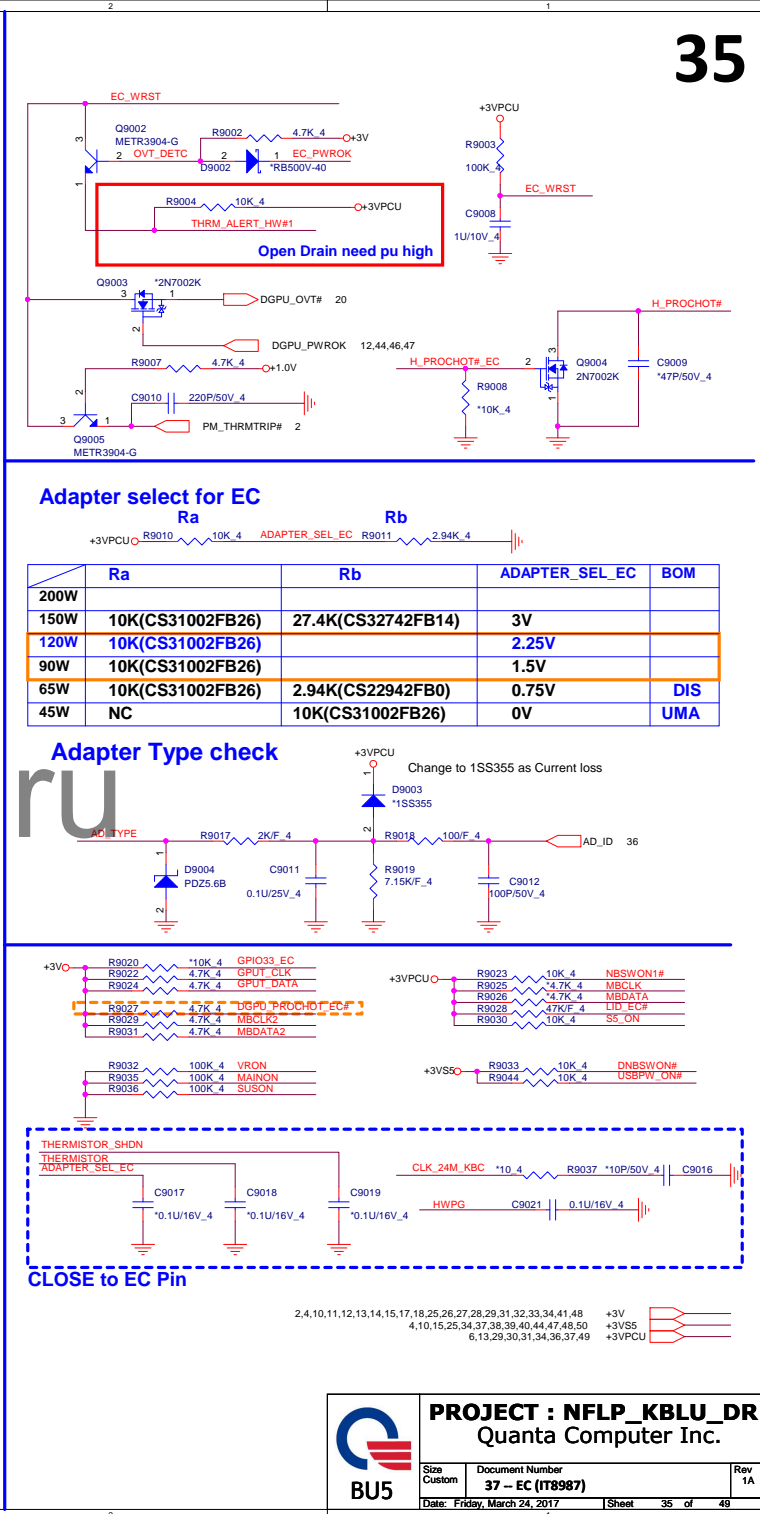
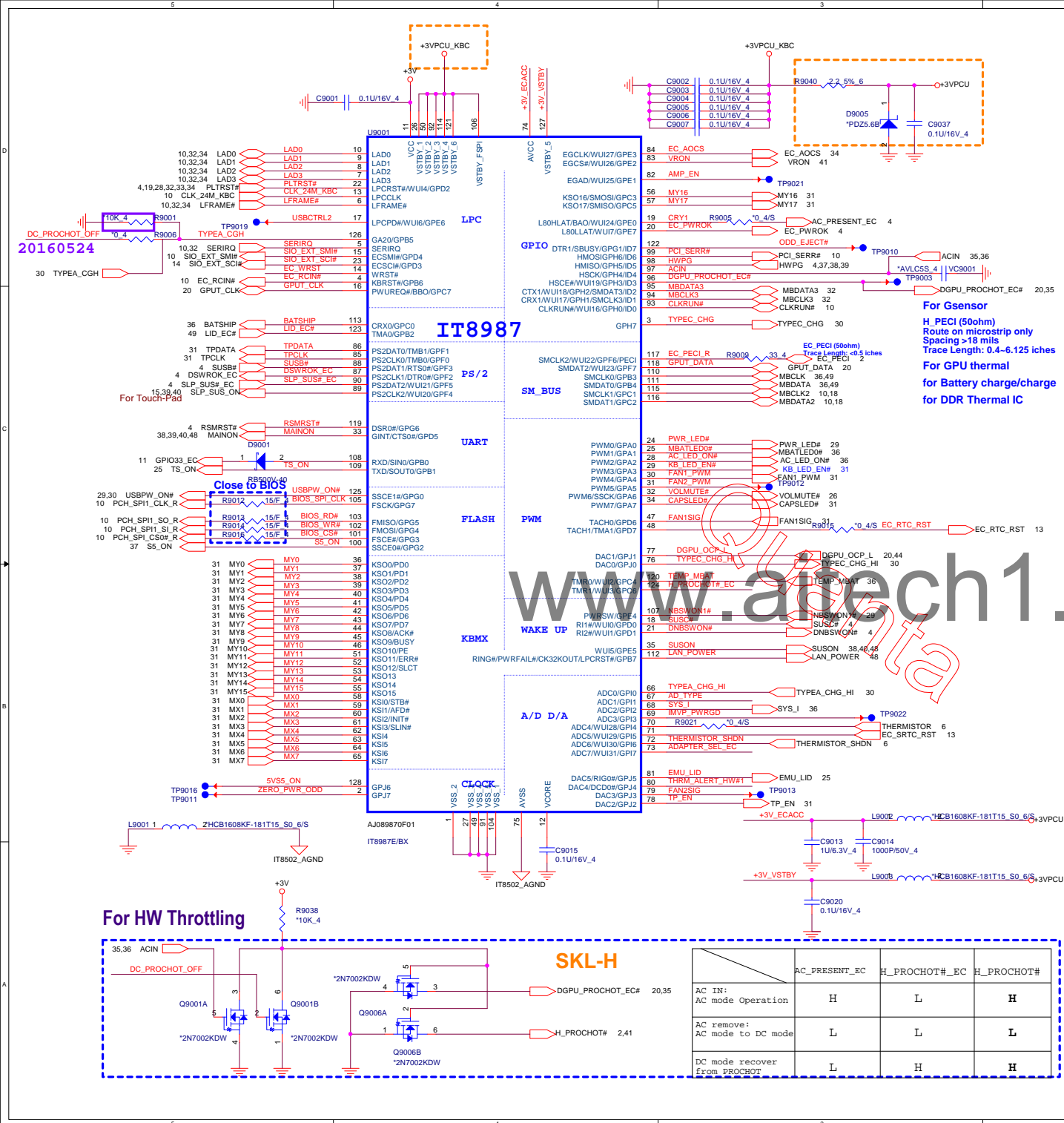
Mini Card  
WLAN/BT(Optional)

## Support Wake Function(Reserve)

0302 Reserved the MOSFET at CLKREQ#  
even the current leakage test passed  
for HP requested

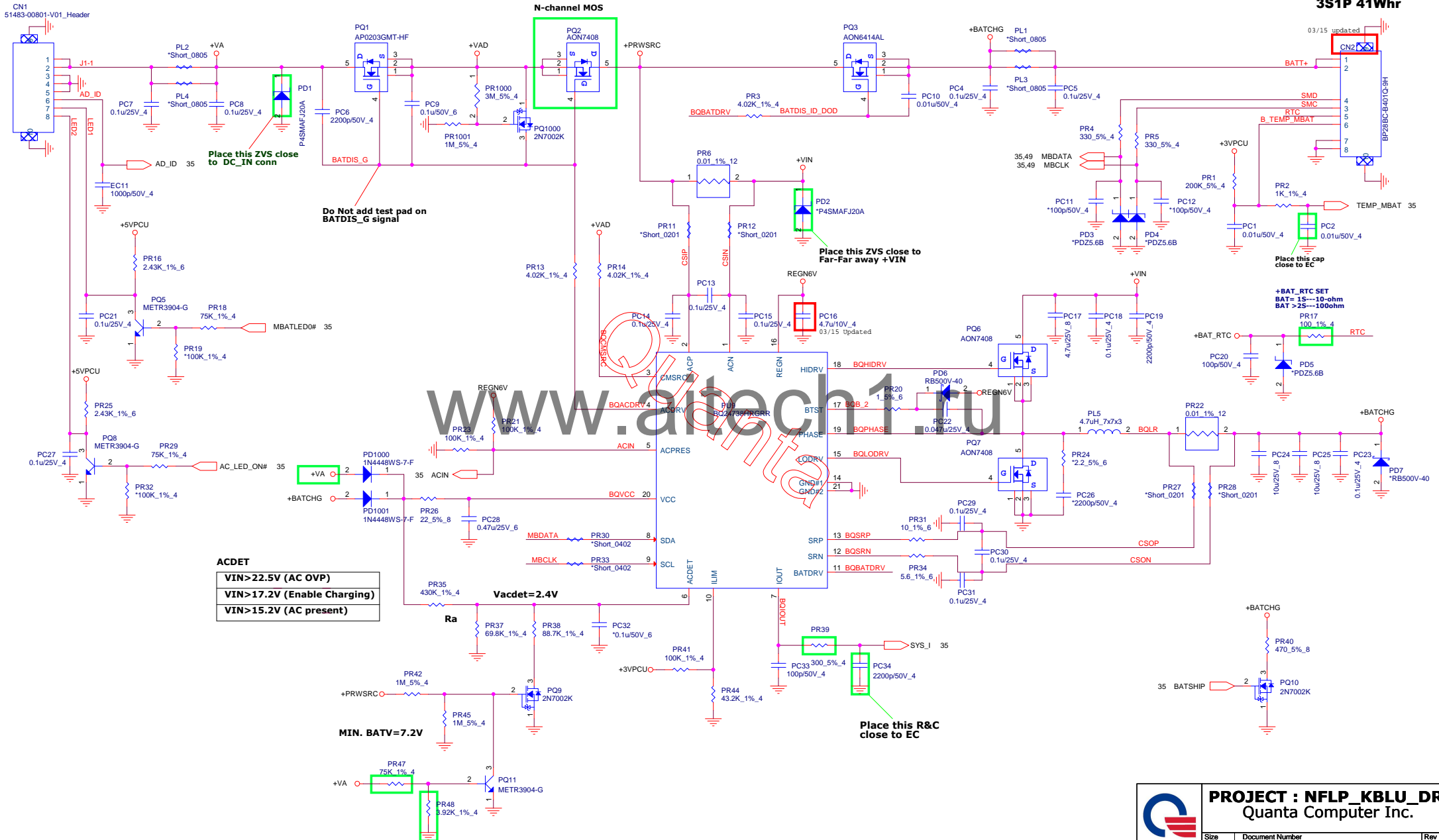
## For EMI Suggestion





ADP=65W

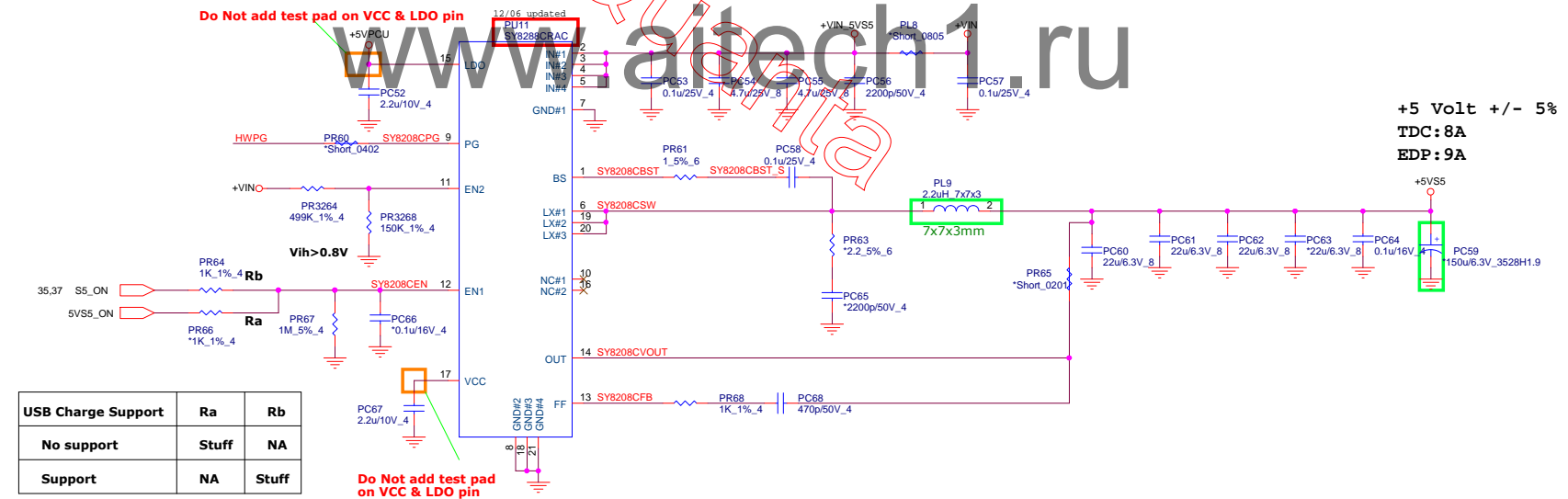
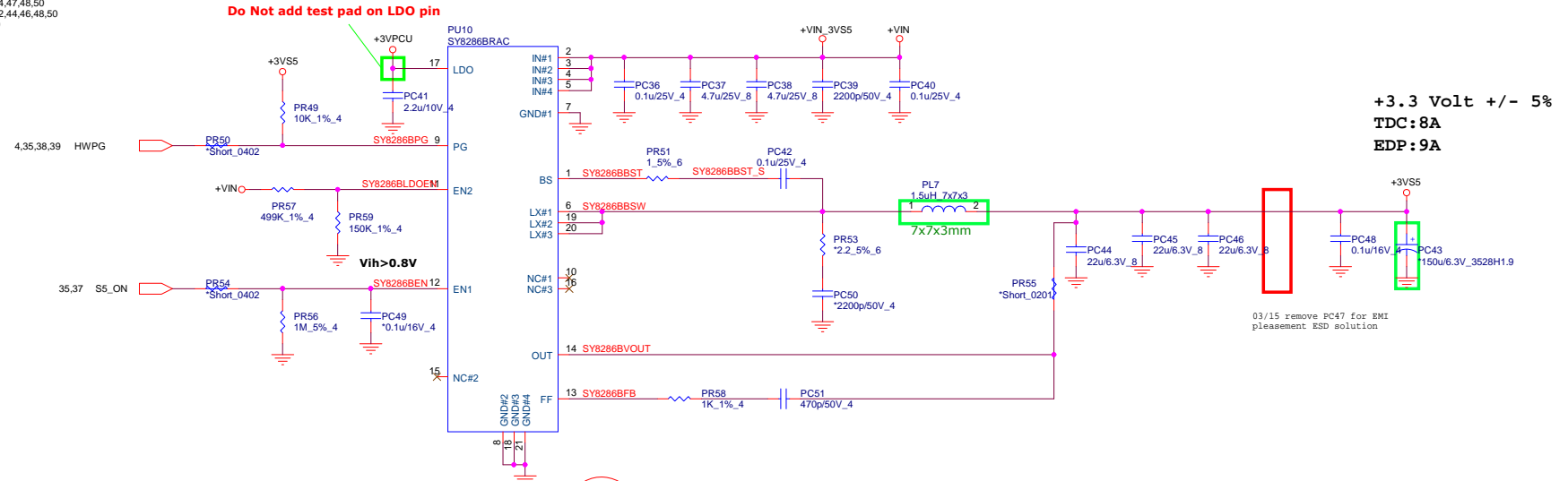
3S1P 41Whr



**PROJECT : NFLP\_KBLU\_DR**  
 Quanta Computer Inc.

Size Custom	Document Number Charger (BQ24738H)	Rev 1A
Date: Friday, March 24, 2017	Sheet 36 of 51	

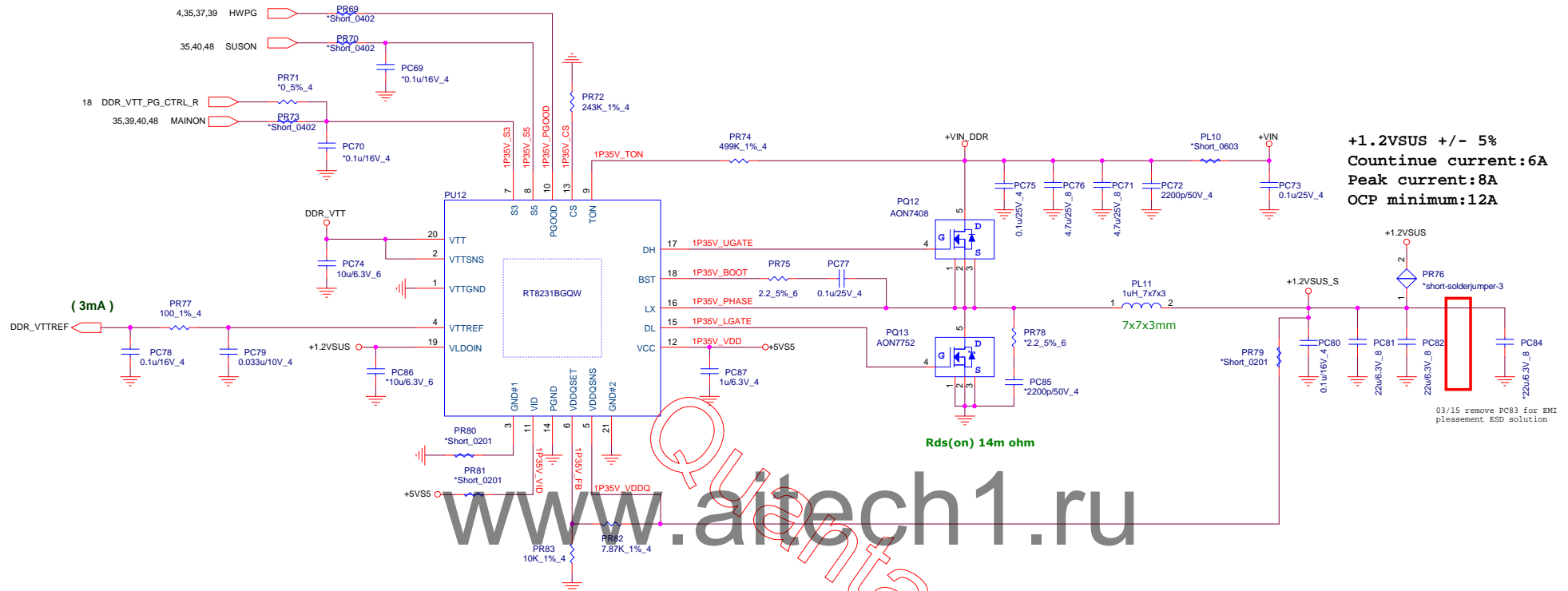
+VIN 25,31,36,38,39,42,43,44,45,46,50  
 +3VS5 4,10,15,25,34,35,38,39,40,44,47,48,50  
 +5VS5 4,25,29,30,38,39,40,41,42,44,46,48,50  
 +3VPCU 6,13,29,30,31,34,35,36,49  
 +5VPCU 26,36,47,48



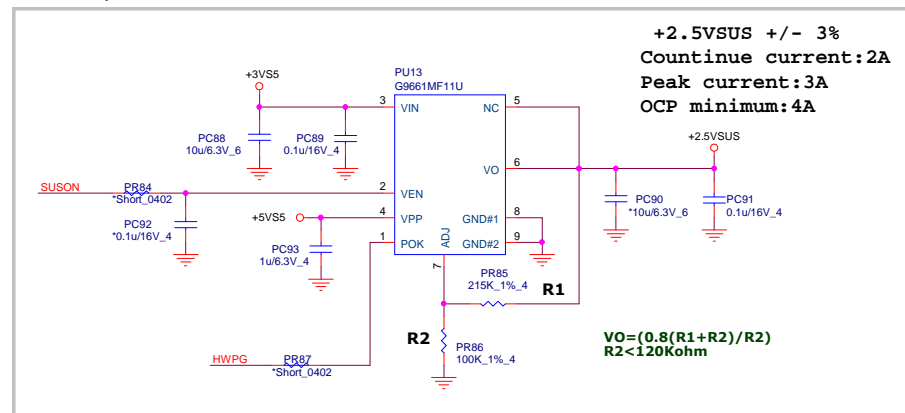
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

**Do Not add test pad on VCC & LDO pin**

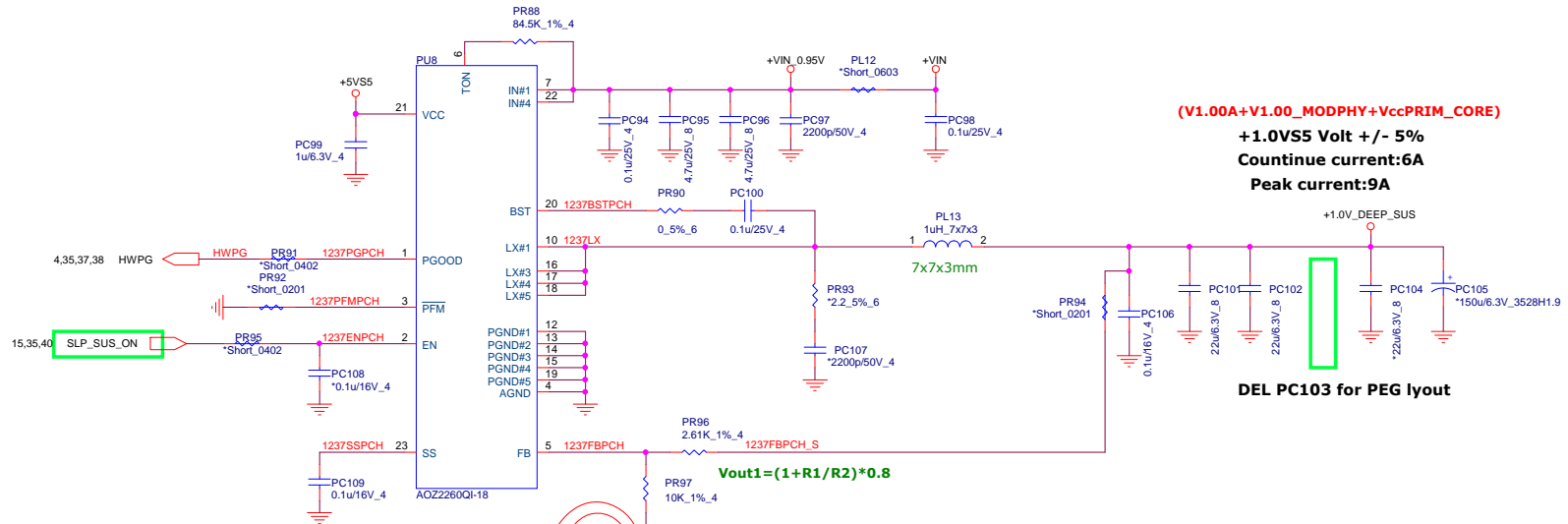
+VIN 25,31,36,37,39,42,43,44,45,46,50  
 +5VS5 4,25,26,29,30,37,39,40,41,42,44,46,48,50  
 +1.2VSUS 3,6,17,18,40  
 DDR\_VTT 17,18



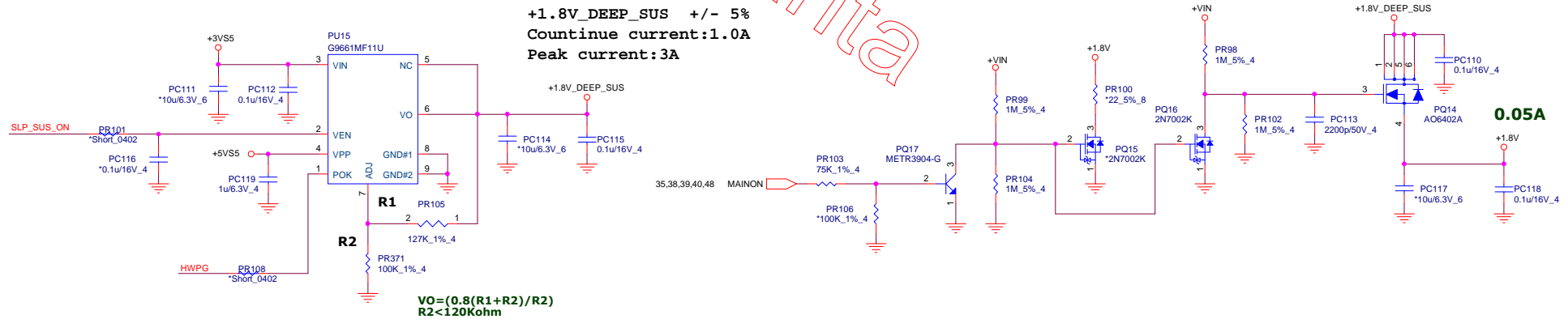
20151015 updated



+VIN 25,31,36,37,38,42,43,44,45,46,50  
 +3VS5 4,10,15,25,34,35,37,38,40,44,47,48,50  
 +5VS5 4,25,26,29,30,37,38,40,41,42,44,46,48,50  
 +1.0V\_DEEP\_SUS 9,13,15,40  
 +1.8V\_DEEP\_SUS 9,15,47  
 MAINON 35,38,39,40,48  
 +1.5V



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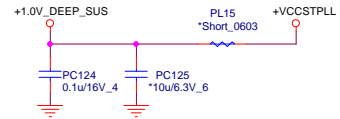


+1.0V 2,4,6,35  
 +3VSS 4,10,15,25,34,35,37,38,39,44,47,48,50  
 +5VSS 4,25,26,29,30,37,38,39,41,42,44,46,48,50  
 +VCCIO 2,6  
 +1.2VSUS 3,6,17,18,38  
 +VCCSTPLL 2,4,5,6,9,41  
 +1.0V\_DEEP\_SUS 9,13,15,39  
 +1.2V\_VCCPLL\_OC 6  
 MAINON 35,38,39,48

**Volume Segment**  
**Vcc\_ST: 0.12A**  
**Vcc\_PLL: 0.12A**

**<= 10ms, full load ready**  
**(Vcc\_ST+Vcc\_PLL)**

**Imax:0.24A**

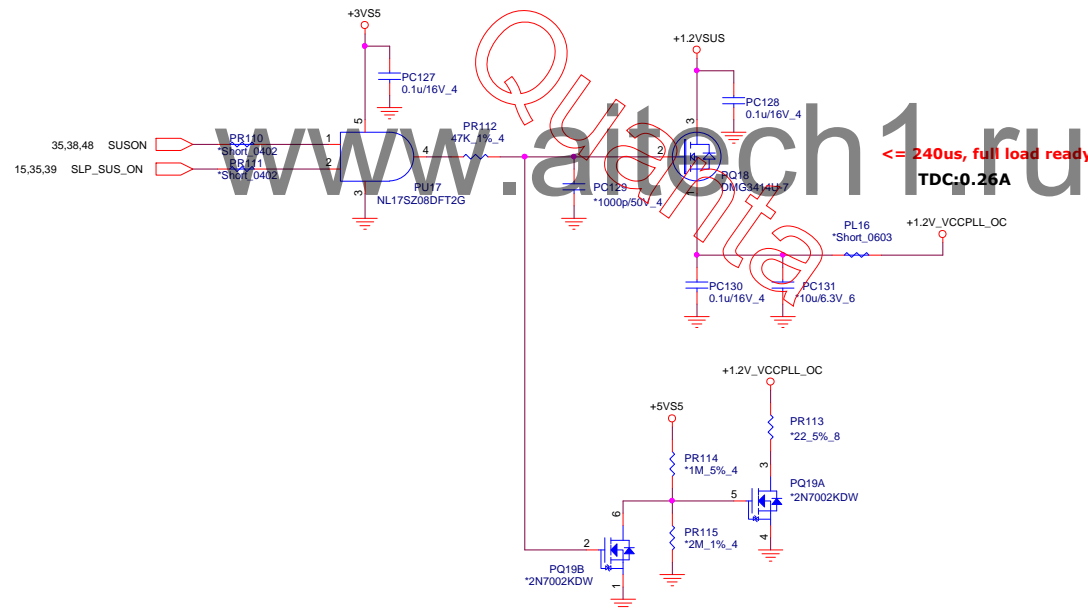
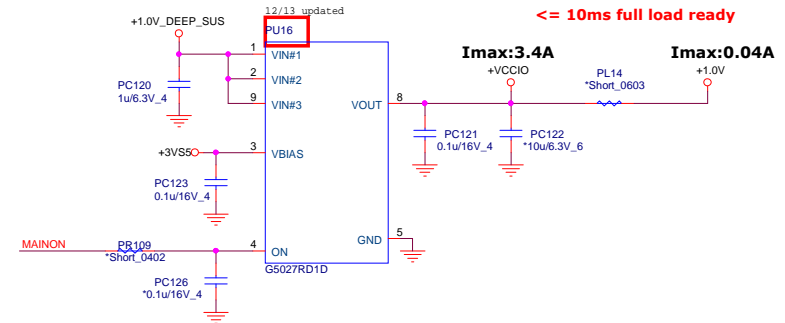


**Volume Segment**  
**Vcc\_STG: 0.04A**  
**Vcc\_IO: 3.4A**

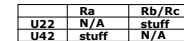
**<= 10ms full load ready**

**Imax:3.4A**

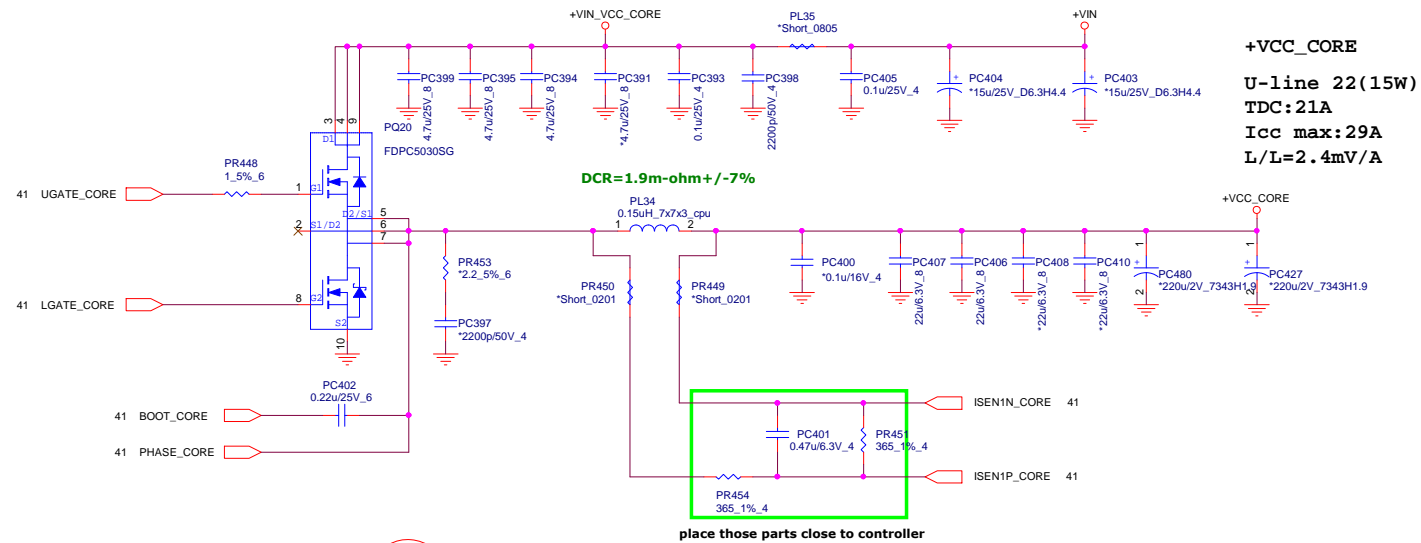
**Imax:0.04A**



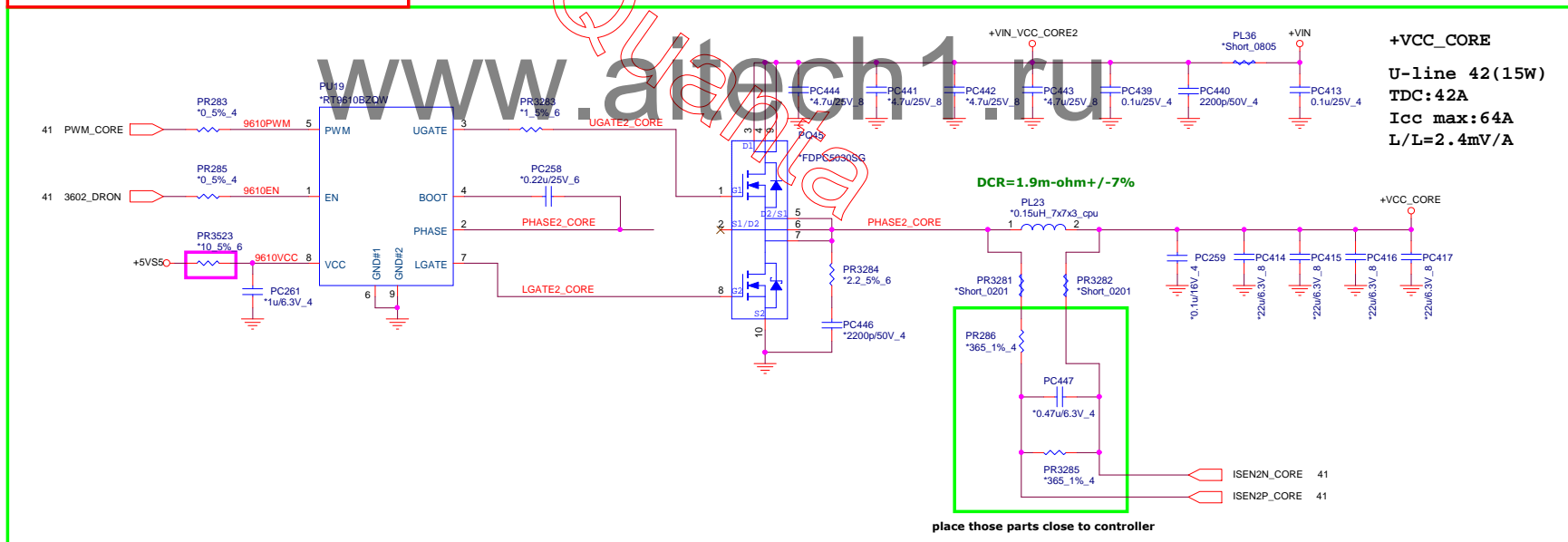
**<= 240us, full load ready**  
**TDC:0.26A**



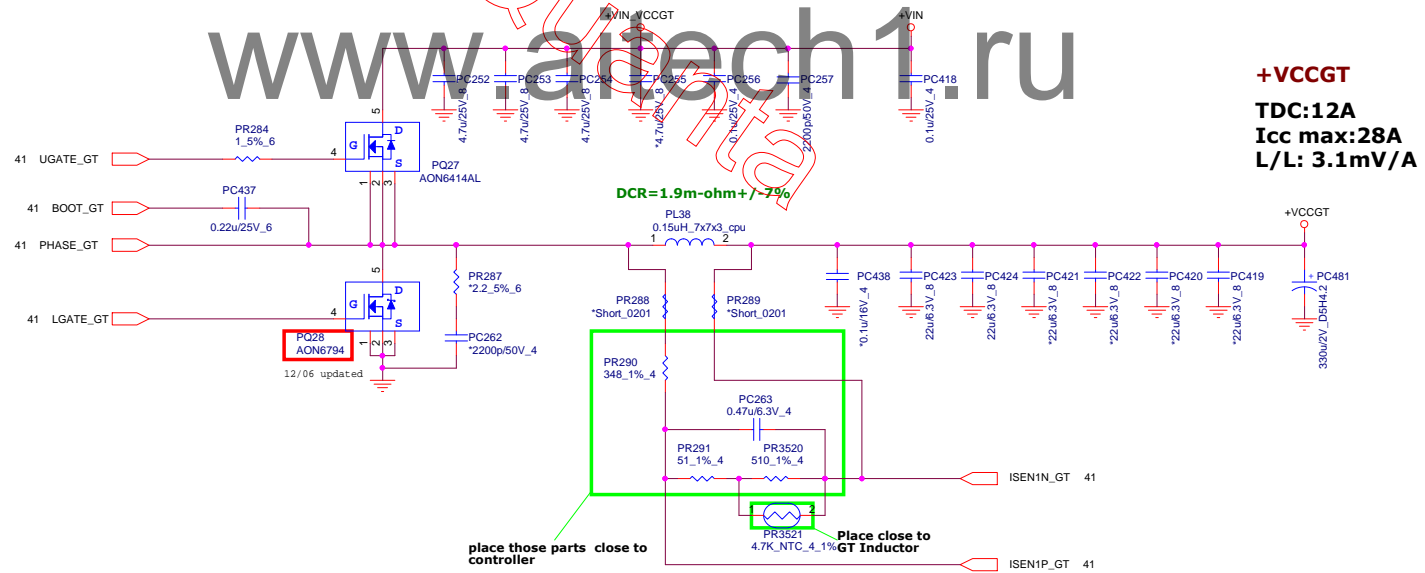
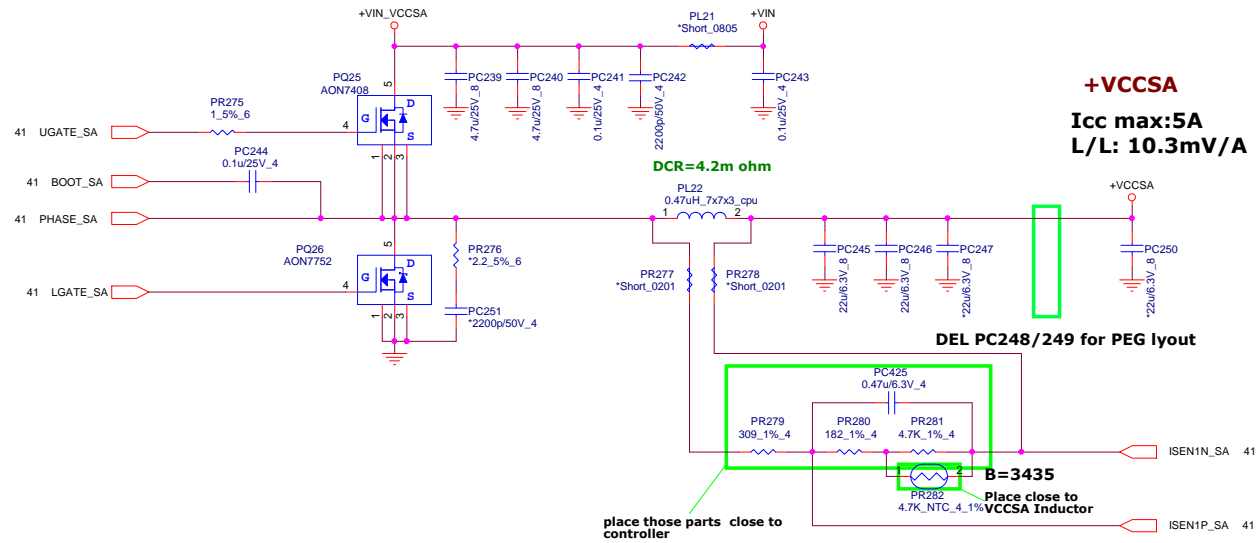
+VIN 25,31,36,37,38,39,43,44,45,46,50  
+5VSS 4,25,26,29,30,37,38,39,40,41,44,46,48,50



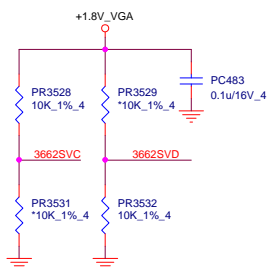
For U42 --> Add These Components



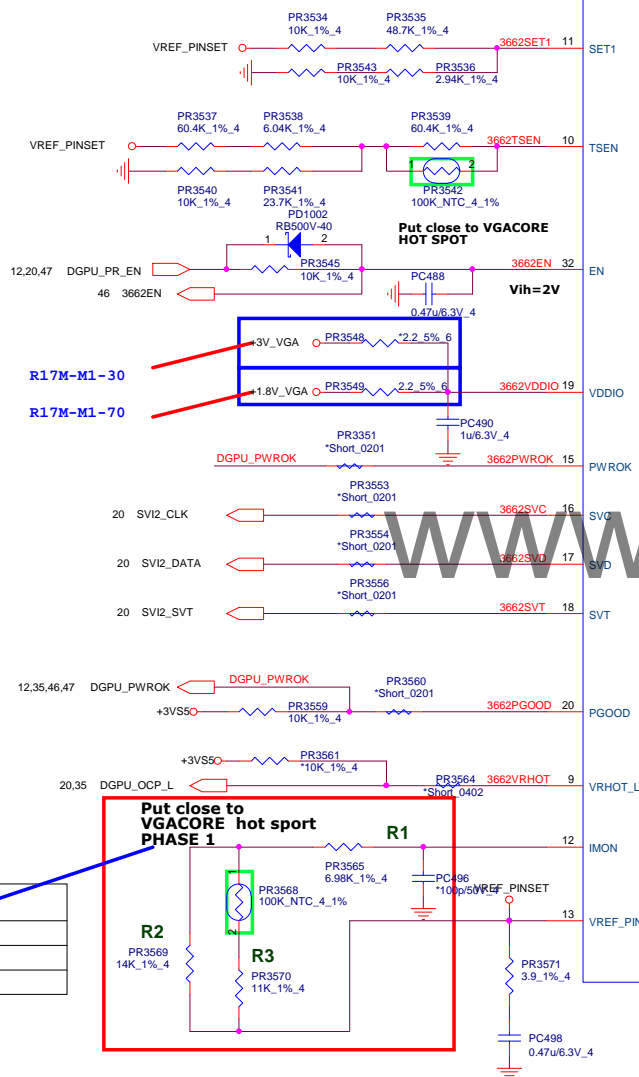
+VIN 25,31,36,37,38,39,42,44,45,46,50  
 +5VS5 4,25,26,29,30,37,38,39,40,41,42,44,46,48,50  
 +VCCSA 6,41  
 +VCCGT 7,41



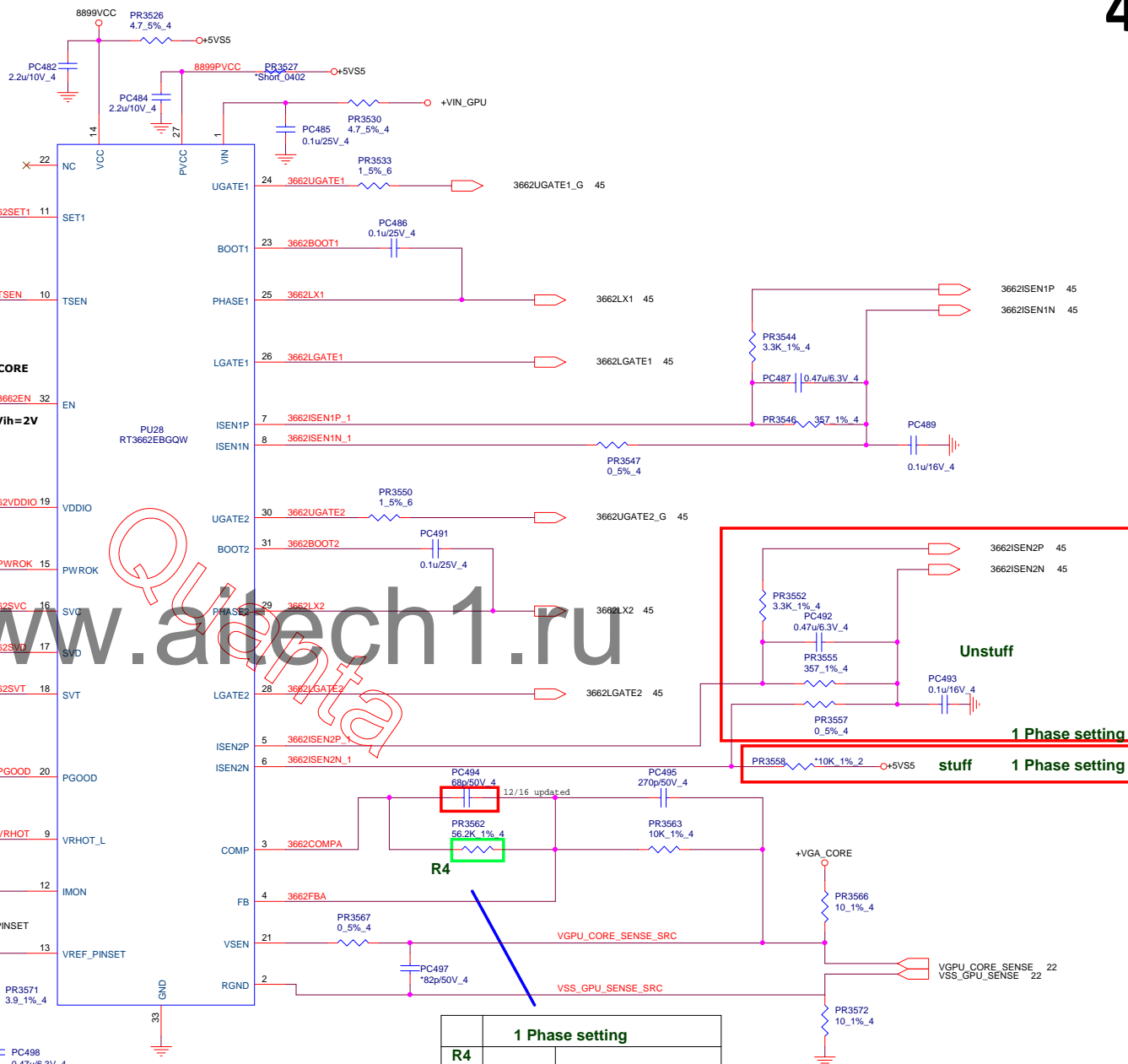
R17M-M1-70



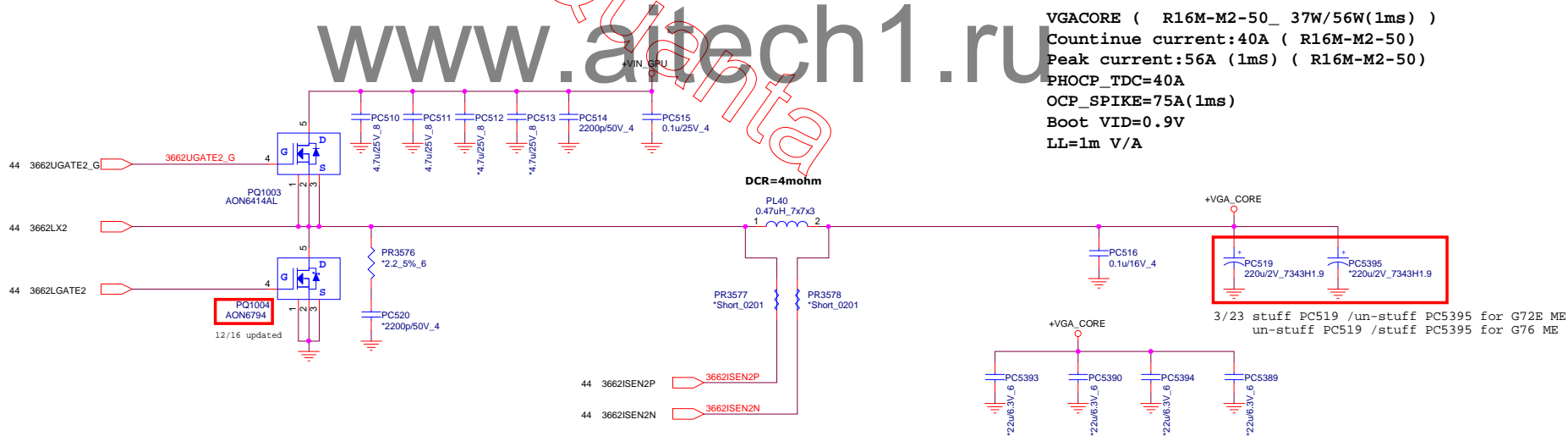
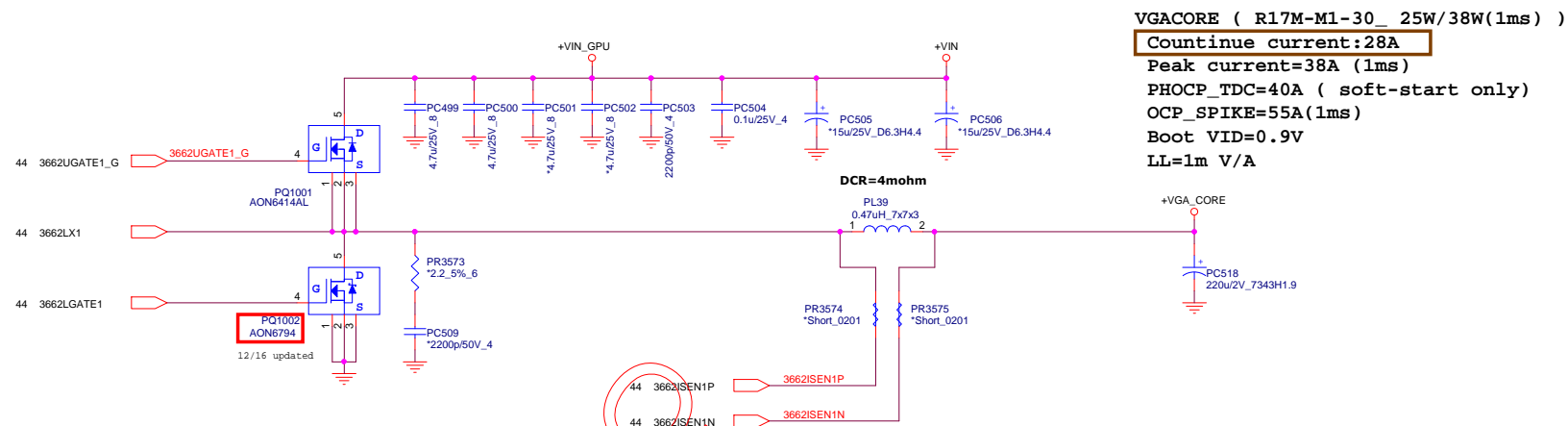
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

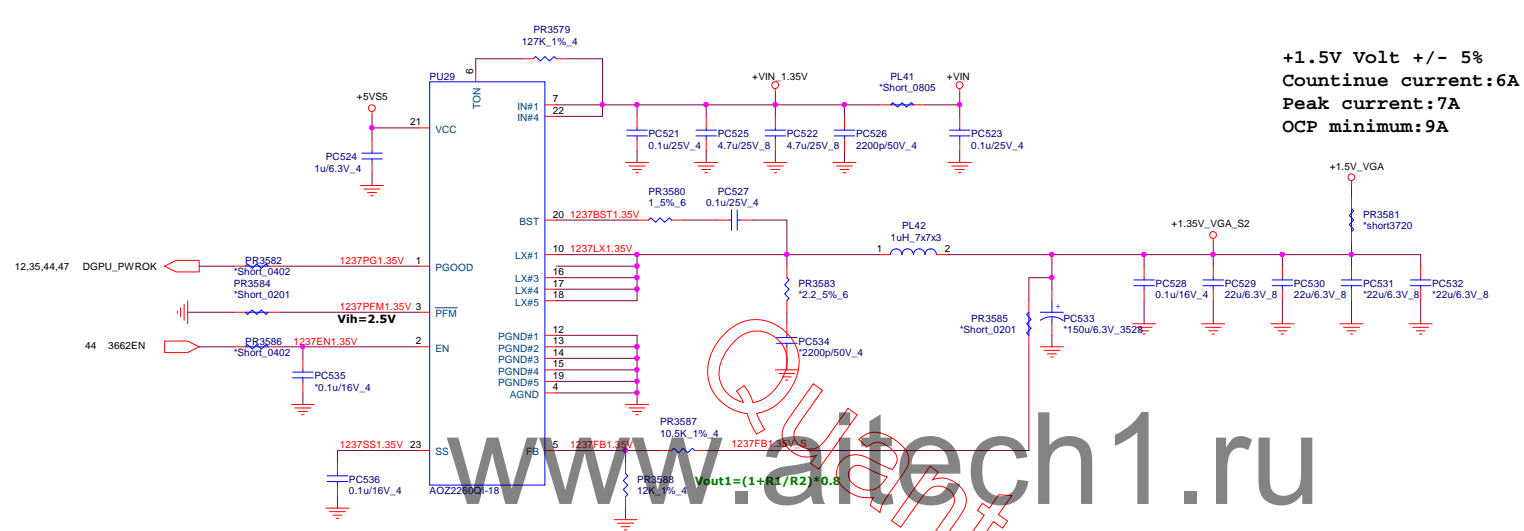


	1 Phase setting	
R1		
R2		
R3		



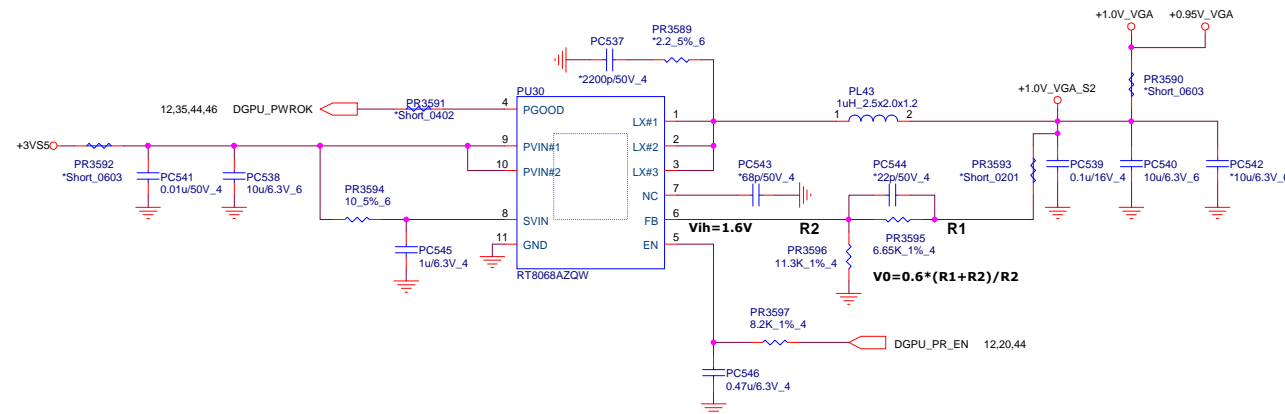
	1 Phase setting	
R4		



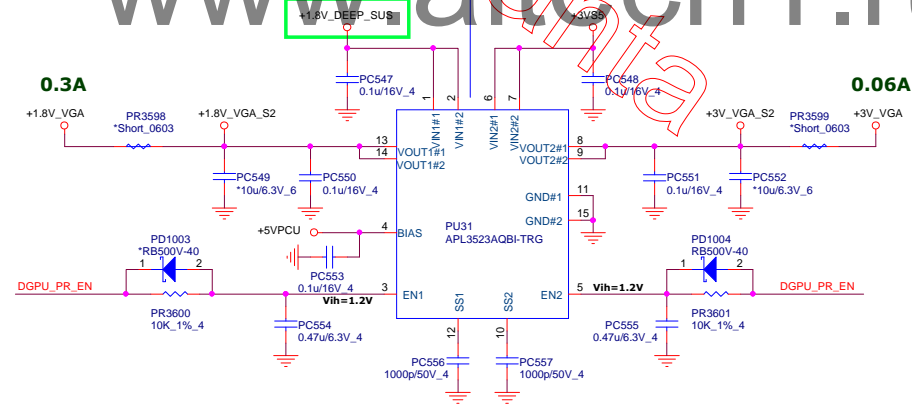


Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

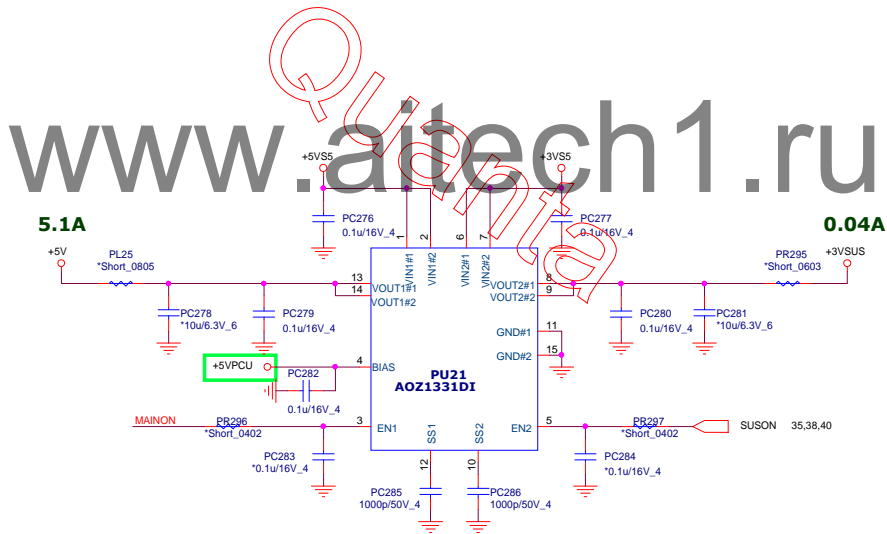
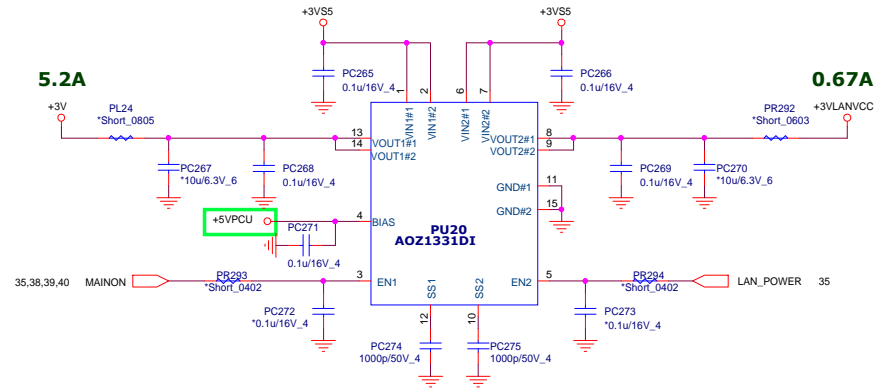
+0.95V +/- 3%  
 Countinue current:2A  
 Peak current:3A  
 OCP minimum:4A



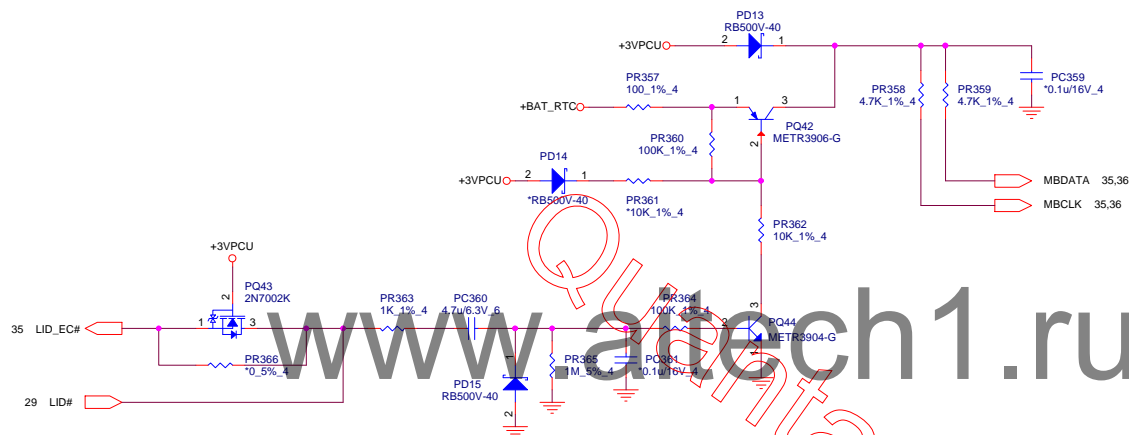
+3V\_VGA  
 +1.8V\_VGA & +0.95V\_VGA  
 +VGA\_CORE & +1.5\_VGA

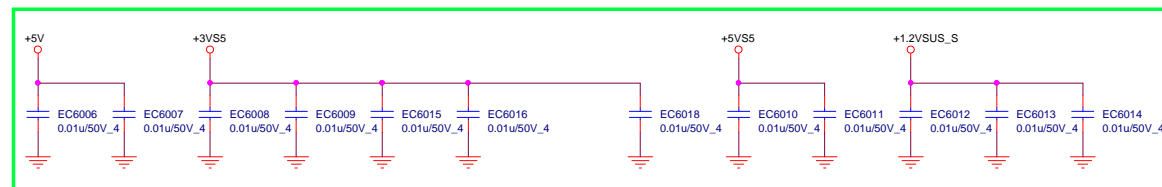
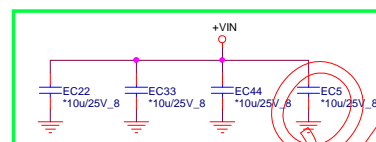
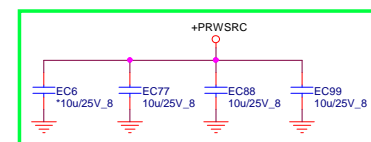


+3V	2,4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41
+5V	25,26,27,31,32,34,50
+VIN	25,31,36,37,38,39,42,43,44,45,46,50
+3VS5	4,10,15,25,34,35,37,38,39,40,44,47,50
+5VS5	4,25,26,29,30,37,38,39,40,41,42,44,46,50
+3VSUS	31
+5VPCU	26,36,37,47
+3VLAVCC	28



+3VPCU 6,13,29,30,31,34,35,36,37  
+BAT\_RTC 4,13,15,29,36



**EMI request for ESD** 03/21 updated**EMI request for ISN****EMI request for ISN**

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